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SCAPE

POWERING E-MOBILITY

D5.1 – Ruggedness & aging analysis of selected power semiconductor devices

SWITCHING-CELL-ARRAY-BASED POWER ELECTRONICS CONVERSION FOR FUTURE ELECTRIC VEHICLES

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Executive Summary

In this deliverable, the ruggedness and aging of power semiconductor devices are analyzed at die level. To this end, a literature review is carried out to identify suitable tests oriented to EV power conversion and linked to the devices degradation and failure mechanisms. Next, the most appropriate tests for multilevel topologies are selected and performed. From the analysis of the results, the most suitable SiC MOSFET references, jointly with other design parameters, i.e., short-circuit actuation time and aging indicators, are provided to ensure a high reliability in the converter. In this sense, the goals of SCAPE deliverable D5.1 entitled “Ruggedness & aging analysis of selected power semiconductor devices” are the following:

- i) Reviewing in the literature the most suitable tests for ruggedness and device ageing oriented to EV power conversion, as well as the device degradation and failure physics,
- ii) Identifying the most appropriate ones and adapting them to multilevel topologies,
- iii) Setting up them for SCAPE project, and
- iv) Using all them for selecting the most suitable SiC device for being used in SCAPE from a ruggedness point of view, and
- v) providing other design parameters, i.e., short-circuit actuation time and aging indicators, to ensure a high degree of reliability on the converter.

For efficiency and reliability reasons, devices with better dielectric-semiconductor interface and lower $R_{DS(on)}$ values at nominal operation conditions have been preferred for the final application. For this reason, the GENESIC device (G4R12MT07-CAU, DUT3) has been selected to be used as a switching device. To enable the actuation of i-fuse an leave time enough for its actuation, the CREE, 1200 V/36 A SiC MOSFETs with an $R_{DS(on)}$ of 80 mΩ (C2M00080120D, DUT4) will be a good candidate whether it is compatible with chip embedding process. DUT3 has been desestimated as it presents a higher density of stated in the dielectric and 4H-SiC/SiO₂ interface, as well as stacking faults that degrades the performance of the body diode.



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List of Acronyms and Abbreviations

4H-SiC 4H-politype of silicon carbide	SC Switching cells
BJT parasitic bipolar junction transistor	SCWT Short-circuit withstanding time
DUT Device Under Test	SEM Scanning Electron Microscope.
EV electric vehicle	ShC I Short-circuit type I
HV High-voltage	ShC II Short-circuit type II
JFET Junction field effect transistor	Si Silicon
LV Low-voltage	SiC Silicon carbide
MOSFET Metal-oxide-semiconductor field effect transistor	SiO₂ Silicon oxide
PCT power cycling test	UIS Unclamped Inductive Switching
SBD Schottky-barrier diode	WBG Wide band-gap

List of Variables

C_{DC} capacitors bank	R_{G(off)} gate resistor for turning on the device
C_{GD} gate to drain capacitance	R_{G(on)} gate resistor for turning on the device
C_{GS} gate to source capacitance	R_{onsp} Specific on-resistance ($R_{DS(on)}/\text{area}$)
C_{oss} MOSFET's output capacitance	R_{shunt} coaxial shunt for I_D measurement
C_{riss} reverse transfer capacitance	R_σ ShC circuit parasitic resistance
E_{ava} Avanlanche energy capability	T_{on} Short-circuit duration, fixed by the circuit
E_{sc} Energy safe curve	t_{shc} Short-circuit withstanding time by the dev
I_{ava} Avalanche current peak	V_{br} breakdown voltage
I_{D,sat} Peak saturation current	V_{BUS} DC bus voltage
I_D MOSFET drain current	V_{DS} Drain to source voltage drop



I_{DSS}	Drain leakage current	V_{GS}	gate to source voltage
I_{GSS}	Gate leakage current	V_{th}	MOSFET threshold voltage
L_{σ}	ShC circuit parasitic inductance	ΔV_{TH}	variation of V_{TH} at different gate voltages with increasing ShC stress cycles
R_b	P base resistance		
$R_{DS(on)}$	MOSFET's on resistance		



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1. Introduction

1.1. Deliverable goals

The goals of SCAPE deliverable D5.1 entitled “Ruggedness & aging analysis of selected power semiconductor devices” are the following:

- i) Reviewing in the literature the most suitable tests for ruggedness and device ageing oriented to EV power conversion, as well as the device degradation and failure physics,
- ii) Identifying the most appropriate ones and adapting them to multilevel topologies,
- iii) Setting up them for SCAPE project, and
- iv) Using all them for selecting the most suitable SiC device for being used in SCAPE from a ruggedness point of view, and
- v) providing other design parameters, i.e., short-circuit actuation time and aging indicators, to ensure a high degree of reliability on the converter.

Among these objectives, several aspects must be clarified. First, it should be pointed out that the ruggedness tests will be oriented to the semiconductor die, without considering the packaging as the switching cells (SCs) are not still manufactured. Notice that thermomechanical tests for packaging aging should be performed with the SC chip embedded technology to be representative of investigation ongoing in SCAPE. Thus, in a second stage, the tests for SiC thermomechanical assessment will be defined and performed during the second year of the project and included in deliverable D5.2 (M24), as described in the proposal. Secondly, although D5.1 clearly concerns the high-voltage (HV) semiconductor devices to be used in the main SCs (traction inverter, battery charger), SCAPE also involves low-voltage (LV) SCs used in the Electric-Vehicle (EV) auxiliary converters. As these converters will not involve chip-embedding processes and their selection is not as critical as for the HV devices, the ruggedness and reliability studies have been focused on SiC power MOSFETs. Obviously, the most suitable references for SCAPE will be selected between those pointed out in deliverable D3.1. Thirdly, ruggedness tests have been performed taking care of the number of available devices during T5.1 execution time until now. Tests have been performed on a reduced number of components, trying to ensure that their suitability is high. Aside from the references selected in T3.1 and presented in D3.1, an additional SiC MOSFET reference (C2M00080120D, 1200 V breakdown voltage) is considered to explore the possibility of its use as an i-fuse as long as it meets with the efficiency requirements of the final application. Finally, it should be indicated that all tests will be adapted from those used in Silicon (Si) Insulated Gate Bipolar Transistors (IGBTs) and in diodes, submitting them under overstress situations typical or representative of EV converters.

1.2. General Overview between Silicon IGBTs and SiC MOSFETs for qualification tests oriented to motor drives

In recent years, there has been a growing interest in silicon carbide (SiC) power metal-oxide semiconductor field-effect transistors (MOSFETs) as a replacement for IGBTs in medium and high bus voltage applications (650 V–6.5 kV), especially for motor drives. SiC MOSFETs offer superior properties, such as high frequency, high efficiency, and high density, which enable the design of power converters with improved performance [1], [2]. The market now offers commercially



available SiC MOSFETs with various breakdown voltage (650–1700 V) and current (5–600 A) ratings from multiple manufacturers. These SiC MOSFETs have undergone several generations of technological advancements, resulting in reduced chip size, specific on-resistance, and temperature sensitivity [3]–[5].

Despite their superior performance compared to Si IGBTs, SiC MOSFETs face challenges related to their ruggedness and reliability due to distinct differences in the properties of SiC and Silicon (Si) materials. Firstly, SiC MOSFETs exhibit a significantly higher density of interface traps at the 4H-SiC/SiO₂ interfaces, which adversely affects their ruggedness and reliability, particularly concerning the gate oxide [6], [7]. Secondly, the wider bandgap of SiC compared to Si results in smaller conduction band and valence band offsets with the gate oxide (SiO₂), leading to increased influence on the Fowler-Nordheim tunnelling current flow into the gate oxide and accelerated degradation of SiC MOSFETs under stress [8]. Thirdly, the high electric field capability of SiC creates higher electric fields in the gate oxide, passivation dielectric, and MOS inversion layer, which can cause the degradation of the MOS inversion layer mobility and on-state resistance [9]. Finally, the higher Young's modulus of SiC material compared to Si introduces stronger mechanical stress into the package of SiC MOSFETs, resulting in shorter estimated lifetimes under temperature cycling or power cycling stress compared to Si IGBTs [10].

Numerous research efforts have focused on investigating the ruggedness and reliability of commercial SiC MOSFETs under harsh conditions oriented to motor drives qualifications. Extensive characterization studies have been conducted to evaluate the endurance capability of SiC MOSFETs under extreme conditions, including Short-Circuit (ShC) and Unclamped Inductive Switching (UIS) stresses [11]–[17]. Such tests have been commonly used for the qualification of Si MOSFETs and IGBTs for such applications, as discussed further on. In general, experimental results indicate that the state-of-the-art of commercial SiC MOSFETs still exhibit weaker ShC capabilities compared to Si IGBTs [11]–[13]. Additionally, the avalanche capability and failure mechanisms of commercial discrete SiC MOSFETs and power modules have been studied under single pulse avalanche stress, revealing that SiC MOSFETs can withstand higher current densities and longer avalanche times compared to Si IGBTs, but certain factors such as chip size, active layer thickness, and process imperfections can counteract the advantages of SiC material, particularly under large inductance conditions [14]–[17].

Furthermore, several investigations have been dedicated to assess the ruggedness of commercial SiC MOSFETs under harsh conditions. While it is expected that SiC MOSFETs can endure harsh stress conditions and operate for longer durations without performance or physical degradation, the performance degradation of SiC MOSFETs under accelerated stress is more significant than that of Si devices. This is primarily due to the larger density of defects within the gate oxide and at the 4H-SiC/SiO₂ interface in SiC MOSFETs [18], [19]. These defects are created as a degradation process, since in comparison to Si MOSFETs, the oxide surface electric field is higher and offers a lower barrier height (2.70 eV vs. 3.15 eV), promoting larger gate leakage currents via tunnel effect [20], [21]. Conversely, the material transition at the 4H-SiC/SiO₂ interface is, from a structural point of view, more complex in SiC substrates [22], [23], increasing the possibility of defects arising during the manufacturing process (e.g., dangling or strained bonds). In any case, all these defects introduce allowed states within the insulator band-gap and are responsible for charge trapping or detrapping processes while the device is under operation. Obviously, this has a negative impact on the device's electrical performance and may even result in its destruction once defects have



percolated the gate dielectric [24], [25]. While the intrinsic gate oxide lifetime of state-of-the-art SiC MOSFETs has improved to over 1 million hours under maximum operation gate voltage [26], the failure rates of SiC devices are still significantly higher, approximately 3–4 orders of magnitude, compared to Si devices [27]. Additionally, the degradation of gate oxide poses a significant challenge for SiC MOSFETs. Repetitive ShC stress, avalanche stress, and surge current stress cause notable deterioration in threshold voltage, drain leakage current, and on-state resistance due to charge tunnelling into the gate oxide [28]–[30]. Previous studies have investigated the package reliability of SiC MOSFETs using power cycling test (PCT) and temperature cycling test [31]–[33].

According to all stated here, the tests identified to qualify power devices ruggedness in motor drives will be presented and described in the next section. This review will not be only focused on components with a breakdown voltages ranging from 600 V to 750 V, but also others with 1200 and 1700 V. In the literature, there is a lack of information on the components belonging to 600 V–750 V breakdown voltage range and a link with the results obtained here will be done with those reported in 1200 V.

2. SiC MOSFET's Ruggedness & Reliability: State of the art

2.1. Standard tests for Ruggedness & Reliability in motor drives

2.1.1. Ruggedness in SiC Power MOSFETs

2.1.1.1. Short-circuit tests

The ruggedness of SiC MOSFETs against short-circuit (ShC) events is a major concern in power electronics systems, especially in motor driving applications. During a ShC, SiC MOSFETs must endure high current and DC bus voltage until protection circuits activate and gate control signals shut down. Therefore, the characterization of SiC MOSFETs under ShC conditions is important to determine their endurance and assess safety margins in converter designs. The most commonly used test for ShC characterization is the Hard Switch Fault (ShC type I or ShC I), even though it is less demanding than the Fault Under Load (ShC type II or ShC II) test. In a ShC I condition, the Device Under Test (DUT) is activated under faulty conditions, experiencing ShC current and withstanding DC voltage until failure occurs within a certain time (t_{shc}). The goal is to evaluate whether the ShC duration (T_{on}) is sufficient to detect the ShC condition, initiate shutdown, and prevent converter failures. Typically, the fault detection time is estimated to be below 6 μ s, but a margin is usually considered. Comparatively, 1200 V SiC MOSFET discrete devices have shown lower ShC endurance than Si IGBTs. This is attributed to the smaller chip size and higher power density of SiC MOSFETs. Consequently, addressing ShC issues in SiC MOSFETs is crucial for further performance improvement. This includes understanding their characteristics, related circuit and device limitations, classified failure modes, and corresponding failure mechanisms.

The ShC capability of SiC MOSFETs is primarily influenced by the basic cell design/technology, DC bus voltage, and maximum gate drive voltage. When subjected to ShC conditions, significant power dissipation leads to self-heating of the device. The junction temperature during ShC stress depends on the power dissipation, which is mainly determined by the DC bus voltage (V_{BUS}) and peak saturation current ($I_{D,sat}$). The peak saturation current of SiC MOSFETs during ShC is strongly affected by the maximum gate drive voltage. Consequently, t_{shc} and corresponding energy safe curve (E_{SC}) of SiC MOSFETs depend on the maximum gate drive voltage and DC bus voltage.



Additionally, the gate structure of SiC MOSFETs plays a crucial role in their ShC capability, as discussed further on in 2.1.1.2.

Essentially, two failure modes have been reported based on the measured impedances between the gate and drain/source terminals of failed SiC MOSFETs [34]:

- (i) **Failure mode I**, known as gate dielectric breakdown, occurs when the gate terminal is shorted to the source terminal while the drain–source PN junction remains blocking. This failure mode is not observed in Si devices. The failure mechanism of gate dielectric breakdown in SiC MOSFETs involves a deformation of the aluminum and poly-silicon layers, along with cracks in the gate interlayer dielectric (SiO_2). The dissimilar coefficients of thermal expansion between these layers cause thermal-mechanical stress under high temperatures induced by ShC, leading to deformation and cracks. The increased junction temperature during ShC causes aluminum to melt and diffuse into the cracks, resulting in a short between the gate and source terminals. t_{shc} typically ranges between 3–5 μs . To enhance the ShC capability of SiC MOSFETs limited by gate dielectric breakdown, selecting a source metal with a higher melting point and smaller thermal expansion mismatch between the interlayer dielectric and source metal is recommended.
- (ii) **Failure mode II**, also referred to as thermal runaway, occurs when all three terminals of the device are shorted. The distribution of failure modes in SiC MOSFETs is significantly influenced by the maximum gate drive voltage and DC bus voltage. Thermal runaway is a common failure mode observed in Si devices and is characterized by a high off-state drain leakage current that increases rapidly after device turn-off. This is caused by the increase in junction temperature, resulting in a higher intrinsic carrier density and thermal generation current in the drift region. When the maximum junction temperature surpasses the critical limit, the intrinsic carrier concentration exceeds the background doping concentration, causing the device to lose its blocking capability and enter into thermal runaway [12]. Another possible failure mechanism is the activation of parasitic transistors in the SiC MOSFET, where large hole currents activate the parasitic bipolar junction transistor (BJT), leading to increased drain current and the formation of hot spots in the SiC MOSFET die [13].

To illustrate the relationship of these failure modes to the electrical conditions, Figure 1 plots for a 1.2 kV/12.5 A CREE SiC MOSFET (C2M0120160D), the dependence of t_{shc} and E_{sc} on V_{DC} at room temperature and several V_{GS} values [34]. Failure mode I is associated with a high maximum gate drive voltage (e.g., equal or higher than 16 V), while failure mode II is linked to a high DC bus voltage (800 V). Intermediate DC bus voltages (600 V) result in both failure modes. Notice that in both modes, the destruction is activated by thermomechanical or thermally-driven processes, slightly different to what occurs in Si IGBTs, as it can be inferred from Figure 2 extracted from [36]. Figure 2 schematically shows how the temperature vertical profile is distributed within the component from the cathode to the anode, i.e., from emitter to collector in IGBTs (see Figure 2a) or from source to drain. The metal frontside contacts are also depicted. In the IGBT, a wider drift region is present and the temperature peak is far away from the device topside contact than in the SiC MOSFET, as the latter presents a thinner drift region and the temperature peak is closer to the emitter contact. Together with the thermomechanical mismatch, this difference in the vertical structure between Si IGBTs and SiC MOSFETs justify the differences in the failure modes outlined before. Then, to mitigate this temperature peak in SiC MOSFETs, it is important to reduce the peak current under



ShC events. This can be achieved by a more pronounced JFET effect of the p-body regions or a reduced V_{GS} whether a high efficiency in the final application is not required. Further ideas as presented in [29], exist. However, all of them have a negative impact on the on-resistance. Thus, a deep understanding of the system requirements and behavior is needed to derive potential device related measures and system innovations [30] to deal with ShC events while maintaining the extraordinary performance of SiC under nominal operating conditions.

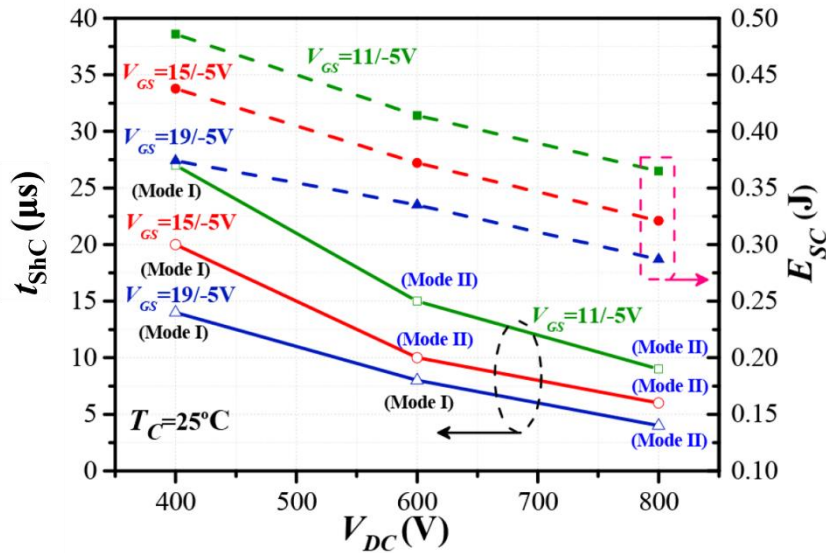


Figure 1 – ShC capability of a 1.2 kV/12.5 A SiC MOSFET at several $V_{DS} = V_{DC}$ and V_{GS} , extracted from [34] and [35].

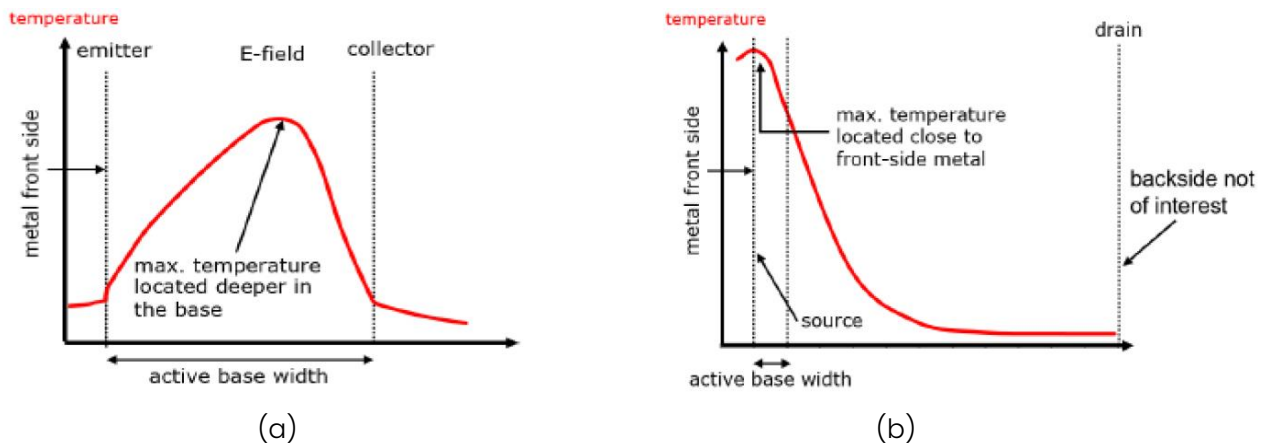


Figure 2 – Differences between heat sources generated during ShC event in: a) IGBTs and b) SiC MOSFETs, extracted from [36].

2.1.1.2. Unclamped inductive switching

SiC MOSFETs have been widely used in high switching frequency applications with inductive loads such as induction motor and fuel injector coil circuit [39]. In these circuits, power semiconductor devices are connected in series with an inductive load or due to the presence of stray inductance, the abrupt change of drain current from the inductive load may force the devices into the avalanche mode operation and damage the device [40]. Since SiC material has high energy bandgap and low intrinsic carrier concentration, SiC devices may be capable of high-temperature operation up to a junction temperature of 300 - 400°C [41]. Although the SiC MOSFETs are intrinsically avalanche rugged [42], it is necessary to determine the maximum avalanche time that



a power device can sustain before failure and the underlying failure mechanism in the applications. Many papers have investigated the avalanche capability and failure mechanism of commercial SiC MOSFETs under single pulse UIS stress [43]-[47].

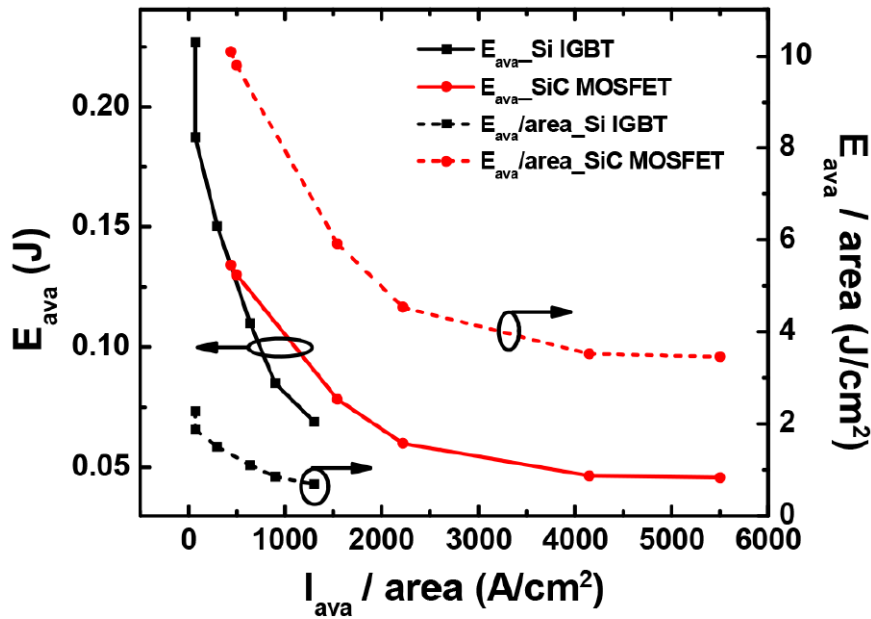


Figure 3 – Avalanche energy capability of 900 V/11.5 A SiC MOSFET and 600 V/16 A Si IGBT [15].

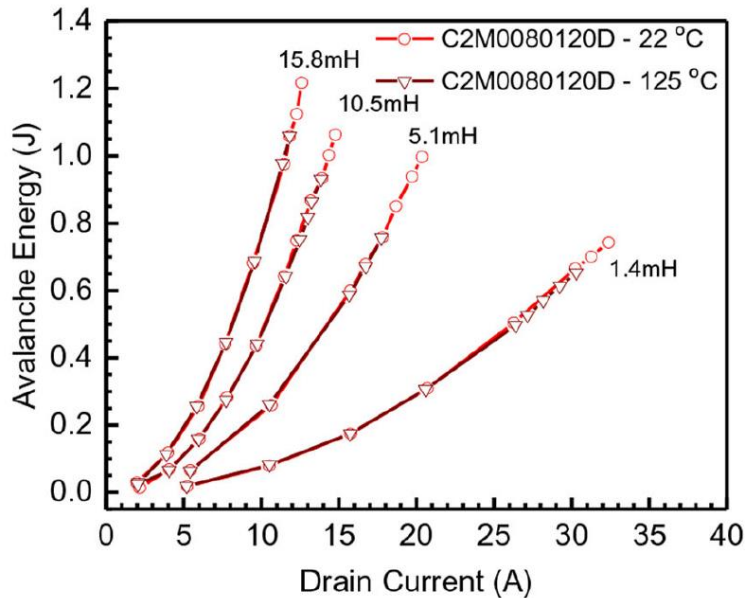


Figure 4 – Avalanche energy of 1200 V/36 A SiC MOSFET under different inductive loads and case temperatures [14].

Figure 3 compares the avalanche energy (E_{ava}) capability of 900 V/11.5 A SiC MOSFET and 600 V/16 A Si IGBT, as well as their avalanche energy density ($E_{ava}/area$), as a function of avalanche current density ($I_{ava}/area$). The same current rating SiC MOSFET and Si IGBT have similar avalanche energy (105 and 104 mJ) at 75 μ H inductance load [15]. The SiC die size is approximately five times smaller than that of the same current rating Si IGBT. From this point of view, the SiC MOSFETs has ~ 3.5 times higher avalanche energy per area capability than Si IGBT. Furthermore, SiC MOSFET can withstand



~20% higher avalanche energy at the same current density 1000 A/cm². Also the SiC MOSFET's avalanche withstand time is longer than Si devices at the same current density [15].

SiC MOSFET UIS tests also have been performed under different inductances, ambient temperatures, and gate voltages to confirm their avalanche robustness [16], [43]. As shown in Figure 4, using a smaller inductance, the avalanche energy and avalanche time duration are smaller due to the higher avalanche current is required to generate sufficient avalanche energy. Using a larger inductance, the avalanche energy is larger. Compared to Si devices, the avalanche capability of SiC MOSFET is insensitive to the temperature. A slight reduction of avalanche duration and avalanche energy has been observed with the increase of temperature [14]. The negative gate turn-off voltage shows a positive influence on the avalanche capability of the SiC MOSFET [43]. The negative turn-off voltage of - 5 V slightly enhances the avalanche withstand capability than zero turn-off gate voltage. It is mainly because a high negative gate turn-off voltage is helpful to keep the MOS channel in the off-state, and it takes a longer time before the onset of source electron current flowing through the channel.

There are two common failure mechanisms during avalanche condition for Si devices, the parasitic BJT latch-up and the attainment of intrinsic semiconductor temperature limit [45], [46]. These two different failure modes may occur when testing with different inductance loads. At large inductance load condition, the avalanche duration time is relatively long, and thereby the device under test has a more uniform heat distribution in the chip, leading to the attainment of intrinsic semiconductor temperature limit during the avalanche stress. When a small inductance is used, the avalanche duration time is short, and there is insufficient time for the chip temperature to rise uniformly, forming local hot-spot and inducing BJT latch-up failure. The parasitic BJT turn ON is mainly influenced by the voltage drop across the P base resistance (R_b). The power dissipation during the avalanche stress increases the junction temperature of MOSFET, thus increasing the R_b because semiconductor resistivity increases with temperature. If the current flowing across R_b can lead to a sufficiently large voltage drop across the base-emitter of the parasitic BJT, it can induce latch-up of the parasitic BJT. The parasitic BJT of SiC MOSFETs is difficult to be triggered due to the inherent properties of WBG SiC material, the turn-on knee voltage of SiC P-N junction is ~3 V at room temperature, which is four times higher than Si [14]. However, the avalanche mode power dissipation in the SiC MOSFET can cause the lattice temperature to increase beyond the intrinsic limit, at which point the device would lose its drain to source blocking capability and thermal runaway of the device occurs. Therefore, the failure mechanism during avalanche condition for SiC MOSFETs is not the parasitic BJT latch-up, but the attainment of intrinsic semiconductor temperature limit [16]. Another failure mechanism of SiC MOSFETs avalanche breakdown is likely to be degradation of metallisation and dielectric under avalanche stress [47]. High power dissipation in the device may lead to an extremely high temperature, which is higher than the melting point of aluminium but is still smaller than the intrinsic temperature of SiC (about 1700 K). The electro-thermal stress may result in the gate oxide failure and ultimately device destruction.

Since the material used makes SiC MOSFETs more rugged than Si devices and in SCAPE, the SiC MOSFET always will have a diode in antiparallel, the condition of UIS will never be reproduced in this project. This is why it has been decided to focus SCAPE ruggedness studies on ShC events. To link the destruction process in ShC I to the device internal basic cell, a discussion on this sense has been provided in the next section 2.1.1.3.



2.1.1.3. Role of SiC MOSFET basic cell structure in device ShC / ruggedness

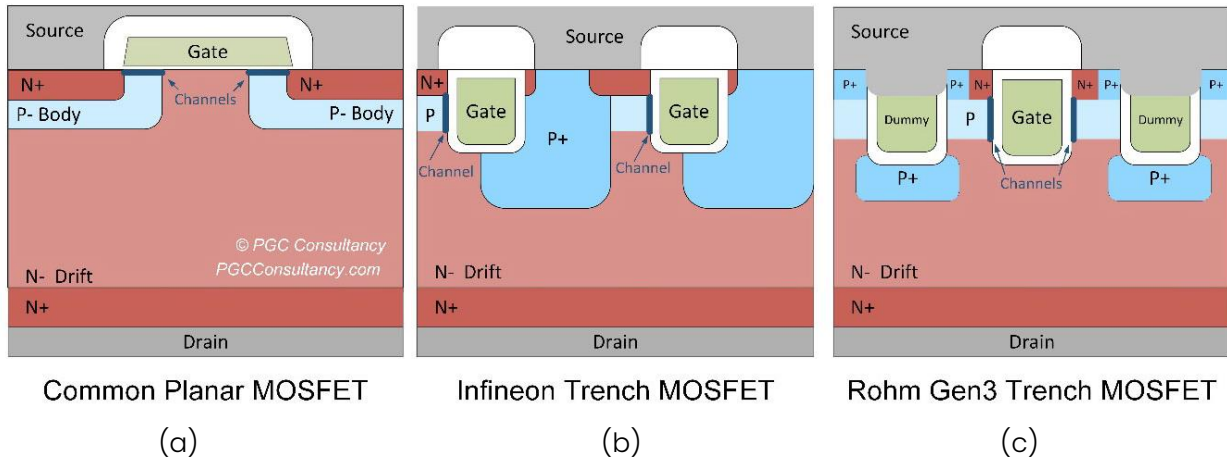


Figure 5 – Technological basic cell structure in currently available SiC MOSFETs and linked to manufacturer: a) Planar MOSFET (CREE, Wolfspeed), b) trench structure with deep high energy implants (Infineon) and c) deep trench etches structure (Rohm) [49]. Source: [Techinsight](#)

From a technological point of view, there are two types of implementation of basic-cell structure, as depicted in Figure 5. Conventional ‘planar’ MOSFETs (see Figure 5a) have their gate and channel region located on the semiconductor surface. Planar MOSFETs are easy to manufacture and fairly reliable. However, to reduce chip size, and hence to improve yield, its lateral topology imposes a limit as to how far, ultimately, it can be shrunk. For instance, CREE and Wolfspeed use this technology. On the other hand, trench MOSFETs (see Figure 5b and Figure 5c) comprise a gate formed on the edge of a trench, that has been etched into the SiC surface. The trench gate is used to create a device with a lower specific on-resistance (R_{onsp} , $R_{DS(on)}/area$). Achieving a lower R_{onsp} allows the chip manufacturer to shrink down the size of the die, thereby utilising less SiC, thus benefitting yields. Multiple reasons lie behind the trench MOSFET’s lower R_{onsp} . First, a gate fabricated on a SiC trench sidewall has a higher channel mobility, meaning electrons are impeded less passing down through a trench gate than compared to the planar device. This reduces the channel resistance. Second, trench MOSFETs can possibly eliminate a planar MOSFET’s JFET resistance, the region in which the current from two channels are squeezed into a narrow passage between the p-body contacts, as occurs in conventional planar devices. However, as we will see, practical, pragmatic design may lead to a JFET-like region being reintroduced. Third, a greater density of vertical trench gates should be possible compared to the number of planar gates, so decreasing cell pitch and increasing current density. Fourth, the lateral sidewalls of the trench can present slightly different threshold voltages as well as significantly different channel mobility, overcoming those of planar devices. In this case, Infineon and Rohm use this technology to produce their MOSFETs. As for GENESIC devices, no details are known about their internal structure, neither can be provided as CSIC has signed a confidentiality agreement with this manufacturer.

The ShC capability of SiC MOSFET is influenced by the gate structure of SiC MOSFET. For a fixed breakdown voltage, V_{DC} value and at a gate voltage between 16 – 20V, the trench gate SiC MOSFETs may be less robust and actually have smaller t_{shc} than the planar gate ones [48]. The E_{SC} is also smaller for trench gate designs in comparison to planar gate MOSFET structures from the same manufacturer. This is due to a further reduction in chip size and a higher power density of trench gate SiC MOSFET, which make them less rugged than planar ones but more efficient. Aside from



this, trench MOSFETs face other challenges when they are optimised for reliable and rugged operation [49]. In particular, successful designs must navigate the problem of maximising SiC's high electric field (9x greater than Si's) at the top of the device, while protecting the delicate gate oxide, which is also located at the top of the device from the same field. This balancing act requires complex device layouts, or otherwise, the drift region will require serious derating, eroding the gains of the trench architecture. A disadvantage of trench MOSFETs is therefore their more complicated design, typically requiring a greater number of fabrication steps, a few of which may have particular complication– deep high energy implants (in the case of Infineon's, see Figure 5b), or deep trench etches (ROHM Gen4's, see Figure 5c).

In the case of Infineon (commercially called CoolSiC MOSFETs), the basic cell is arranged along stripes [50]. Following the considerations presented before, the doped regions adjoining the trench are asymmetric. The left hand side of the trench sidewall contains the MOS channel which is aligned to the a -plane in order to achieve optimum channel mobility (see Figure 5b). A large portion of the bottom of the trench is embedded into a p-type region which extends below the bottom of the trench (see Figure 5b). This p-type region has three main electrical functions [50]:

- i) connect the p-body region to the source electrode as low-resistive as possible,
- ii) form an efficient p-type emitter to operate the body diode as rapid freewheeling diode and
- iii) protect the gate oxide of the trench corner against a too high electric field induced by the drain bias.

This MOSFET structure inherently owns a favorable small ratio of the Miller capacity C_{GD} related to the gate source capacity C_{GS} [50]. C_{GS} is comparably large since a large part of the trench contributes to it, i.e. the n⁺-type areas on both sides of the trench and all p-type areas which are all connected to source. This allows for a well-controlled switching with very low dynamic losses [51]. In particular, this feature is essential to suppress undesirable additional losses caused by a parasitic turn-on in topologies using half bridges. The basic cell structure of Figure 5b is also supportive to realize an adequate ShC capability. The JFET region formed by the adjacent p-emitter regions is not only good to limit the oxide field in the trench corner, but also lowers the saturation current of the device by adjusting the distance between the p-type regions. A smaller distance supports both a lower saturation current and lower field in the gate oxide of the trench corner but causes an additional contribution in the overall on-state resistance due to the JFET. In general, all CoolSiC™ MOSFET products are specified today with up to 3 μ s short circuit withstand time and the specified value is tested 100% on packaged level before shipment [36].

In relation to ROHM's Gen 3rd MOSFET, a more conventional design was chosen compared to Infineon CoolSiC, featuring channels on each side of the gate trench. Dummy trenches were employed on both sides, incorporating deep P-implants to protect the gate trench. Figure 5c highlights the presence of two inactive source trenches between each active gate trench, as well as wide body contacts, which contribute to a larger cell pitch for a trench device. However, when observing this device from a plan view, the seemingly wasteful layout becomes logical. Instead of traditional gate stripes spanning the device in one dimension, the Gen 3 device arranges gates both vertically and horizontally, creating a two-dimensional grid that nearly doubles the gate density per unit area. This concept is similar to Wolfspeed's hexagonal layout, which achieves a 1.3x



increase in gate density. In comparison to the 3rd Generation device, the 4th Generation device exhibits some similarities and notable differences as depicted in Figure 6 [49]:

- i) ROHM maintains the use of a conventional trench MOSFET design, with channels on both sidewalls of the gate trench. However, each gate trench is now flanked by a single grounded source trench on either side, extending twice as deep into the drift region. This design feature enhances gate oxide protection and reduces $R_{DS(on)}$.
- ii) The adoption of a single dummy/source trench per gate trench allows for a 3x reduction in cell pitch. Consequently, the gate density is nearly doubled, in favor of a traditional one-dimensional stripe layout. This modification represents a minimum net increase of 50% in gate trench density per unit area, contributing to the reduction of channel resistance issues that commonly affect other devices. Previous studies have shown that channel resistance can account for up to 30% of the series resistance in a 650V planar MOSFET.
- iii) The substrate has been thinned, resulting in a substantial reduction of this component.

In consequence, switching losses in Gen 4 are reduced due to the decrease in Miller capacitances, as Figure 7 presents. Although the compared dies were not perfectly matched, a significant ~90% reduction in C_{rss} (at rated voltage) and a proportional reduction in C_{oss} , depending on bus voltage, were achieved (see Figure 7a). Second, despite the reduction in die size and the increase in current density, Gen 4th devices exhibit an increased t_{shc} . This, combined with the reduction in derating, provides further evidence of ROHM's significant advancements in the reliability and robustness of their devices, specially in ShC events, as presented in Figure 7b. Then, these improvements enables optimizing the tradeoff between the opposite requirements of $R_{on,sp}$ and t_{shc} , i.e., obtaining the lowest $R_{on,sp}$ and the longer t_{shc} .

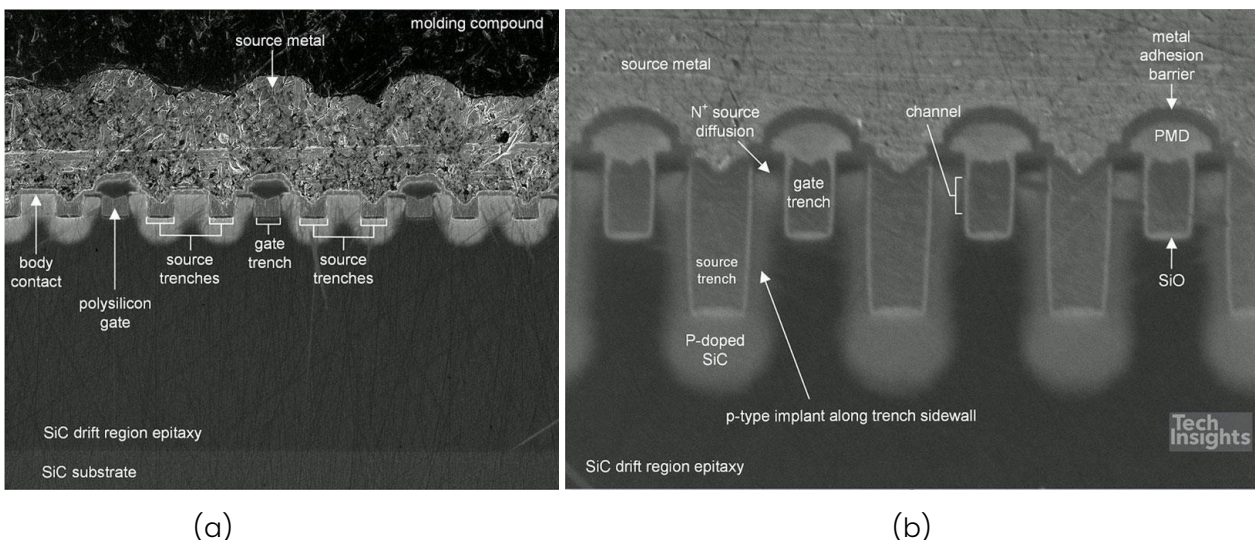
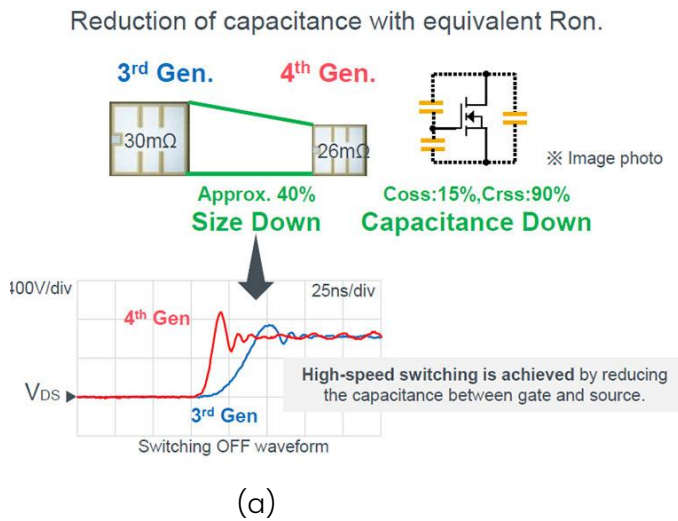


Figure 6 – Technological cut on manufactured SiC MOSFETS: a) Gen 3rd and b) Gen 4th [49] (Source: [TechInsights](#)).



Improved switching characteristics



RonA vs Short Circuit Withstand time

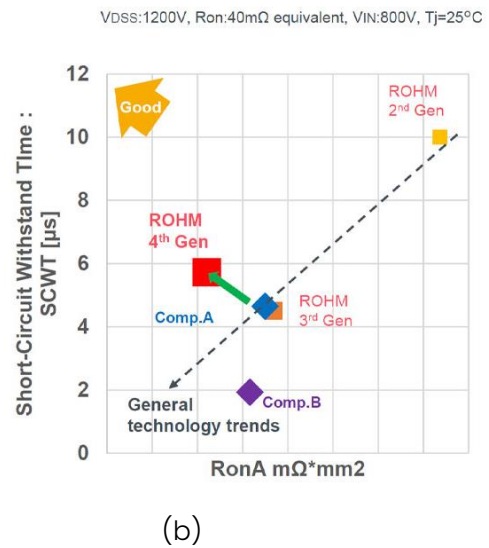


Figure 7 –Changes introduced in Rohm 4th Gen thanks to the new deep trenches: a) size reduction, $R_{DS(on)}$ and switching speed improvement, b) t_{shc} (SCWT in the figure) increased with a lower $R_{on,sp}$ (Extracted from [49])

2.1.2. Device degradation due to repetitive stressful events

2.1.2.1. Degradation under repetitive ShC stress

The determination of the degradation of SiC MOSFETs under repetitive ShC stresses is crucial for ensuring the reliability of industrial applications. Though this problematic will be not investigated in SCAPE, it is interesting including this point in this review for completeness. In this sense, several studies have focused on investigating the effects of long-term or repetitive ShC stress on the static performance of SiC MOSFETs [52]–[55]. Various electrical parameters, including $R_{DS(on)}$, V_{TH} , I_{GSSr} , and I_{DSS} , are regularly monitored during ShC pulse stress. It has been observed that $R_{DS(on)}$ and V_{TH} exhibit a noticeable increase with the number of ShC cycles [28], [55]. This increase is attributed to the melting and reconstruction of the aluminium surface metallization, which leads to higher $R_{DS(on)}$. Additionally, SEM (Scanning Electron Microscope) images of the contact region reveal the formation of significant voids between the aluminium surface metallization and the source contact, resulting in a substantial reduction in the contact interface area [52].

Apart from surface metal deterioration, gate oxide degradation is identified as the primary failure mechanism in SiC MOSFETs under repetitive ShC stress. The shift in V_{TH} is caused by the trapping of charges in the SiC/SiO₂ interface traps. The concentrated flow of ShC current through the MOS channel generates high temperatures in the JFET region located just below the gate oxide. The most affected area is found along the SiC/SiO₂ interface in the MOS channel region. TCAD simulation results indicate that both the impact ionization rate and the perpendicular electric field in the channel region reach peak values during ShC [28]. The impact ionization generation rate and perpendicular electric field at the SiC/SiO₂ interface are positively correlated with the drain-source voltage. Higher maximum gate voltage and DC bus voltage result in more trapped electrons in the gate oxide. The variation of V_{TH} (ΔV_{TH}) at different gate voltages with increasing ShC stress cycles is illustrated in Figure 8 [28]. It is evident that ΔV_{TH} is more significant as the maximum gate voltage is increased, while there is almost no change in V_{TH} when $V_{DS} = 0 V$.



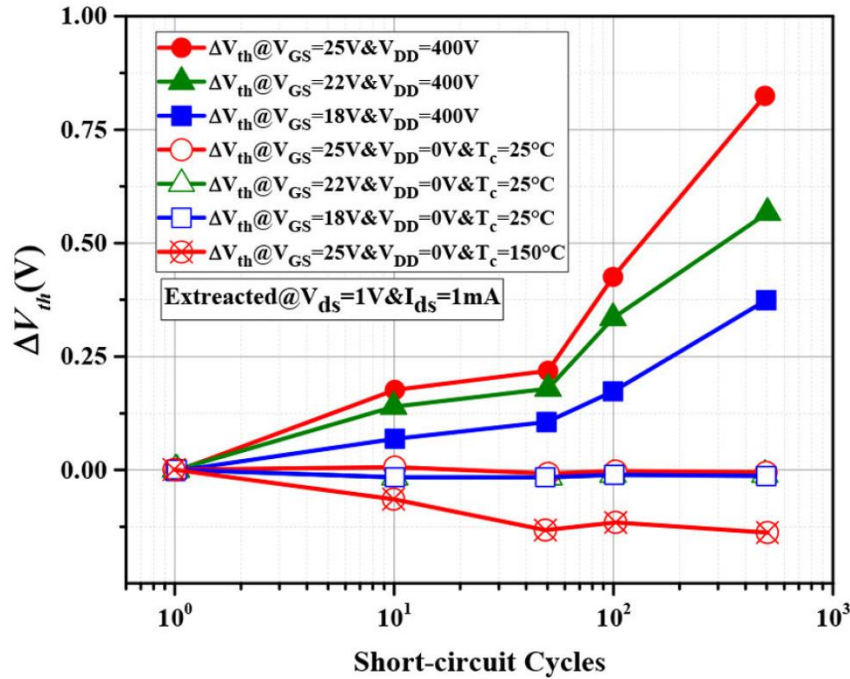


Figure 8 - Variation of the threshold voltage with increasing ShC cycles [28].

2.1.2.2. Degradation under repetitive-pulsed avalanche stress

The electrical performance degradation of SiC MOSFETs under repetitive avalanche stress has been thoroughly investigated. Throughout the avalanche stress test, static electrical parameters are regularly measured at pulse intervals [56]–[58]. Figure 9 illustrates significant deviations of $R_{DS(on)}$, V_{TH} , and I_{DSS} from their initial values after the avalanche stress [57]. Accumulative deterioration is observed within the SiC MOSFETs as the number of avalanche stress pulses increases. Moreover, the parasitic capacitances, including C_{iss} , C_{oss} , and C_{riss} , exhibit an increase following repetitive avalanche stress [58]. This variation in parasitic capacitances leads to an extended turnoff time for the SiC MOSFETs.

To gain a higher insight into this the degradation mechanism, electro-thermal TCAD simulations and microscopy analysis of planar failed devices have been performed in the literature. Simulation analysis revealed that the avalanche current primarily flows through two paths within the MOSFET basic cell. One path flows vertically through the n-drift region and p-body region beneath the source region, while the other path traverses the JFET region and channel region. Although the majority of the avalanche current passes through the internal PN junction of the SiC MOSFET, a small portion flows through the SiC/SiO₂ interface, significantly impacting the static and dynamic characteristics of the SiC MOSFETs [58]. The injection of hot holes into the gate oxide at the JFET region is identified as the primary degradation mechanism for SiC MOSFETs under repetitive avalanche stress [57]. The trapping of holes in the gate oxide above the channel region occurs during the Miller plateau phase, while the injection of holes into the gate oxide above the JFET region predominantly occurs during the avalanche mode phase [57]. These trapping effects along the MOS channel and JFET region contribute to the degradation of V_{TH} and I_{DSS} , but not $R_{DS(on)}$. Upon decapsulation of the failed devices, it was observed that bond wires had lifted off. This bond wire degradation is attributed to thermal fatigue of the material and the disparate coefficients of



thermal expansion within the device after thousands of repetitive avalanche stress cycles, which is considered the main factor contributing to the increased $R_{DS(on)}$.

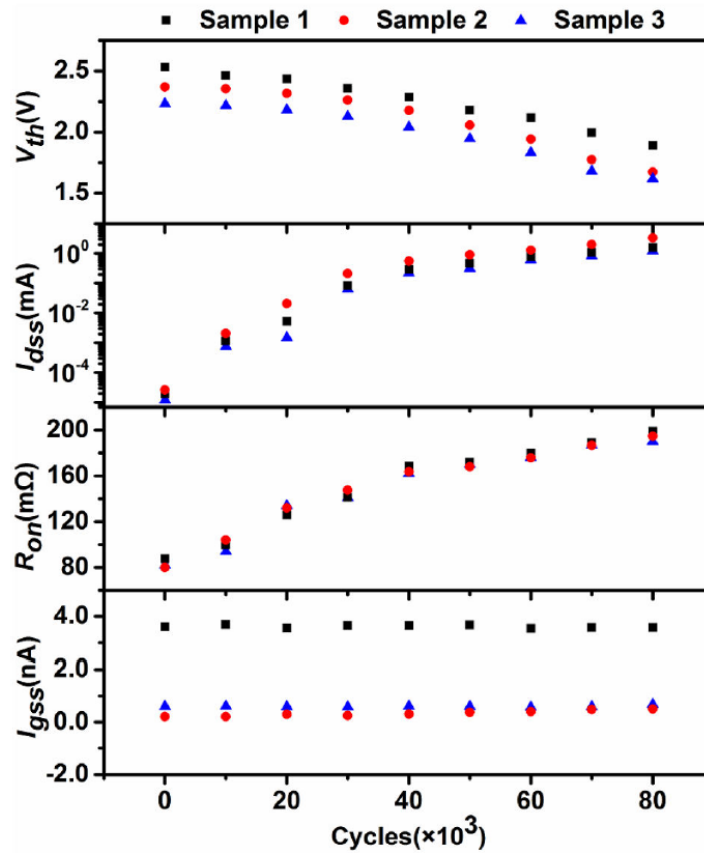


Figure 9. Variations of V_{TH} , I_{DSS} , I_{GSS} , and $R_{DS(on)}$ (referred to as R_{on} in the graph) of the SiC MOSFETs with the increase of avalanche cycles [57].

2.1.2.3. Degradation of body diode under surge current stress

In recent years, numerous studies have explored the viability and advantages of utilizing the body diode of SiC MOSFETs in power applications without an anti-parallel SiC Schottky barrier diode (SBD) [67]–[69]. Operating SiC MOSFETs in synchronous rectification mode without an anti-parallel SiC SBD can achieve almost the same conversion efficiency as conventional inverters that employ SiC SBDs as freewheeling diodes. This is because the external SiC SBD only conducts current during the dead time [69], as it will be the case in SCAPE. However, concerns regarding the reliability and surge current ruggedness of commercial 1200–1700 V SiC MOSFETs' body diodes need to be addressed for converter applications requiring reverse conduction. Long-term converter operation studies have demonstrated the stability of commercial SiC MOSFETs' body diodes over 10,000 hours, with no observed bipolar degradation [70], [71]. Another crucial reliability issue in most applications utilizing synchronous SiC MOSFETs is the surge current capability of the body diode. For instance, the diode must withstand several times the rated current for a short interval during the startup process of power factor correction or specific fault conditions in motor-driven loads [72]. SiC MOSFETs' body diodes exhibit greater surge current capability than SiC junction SBDs of the same current rating [73], [74].



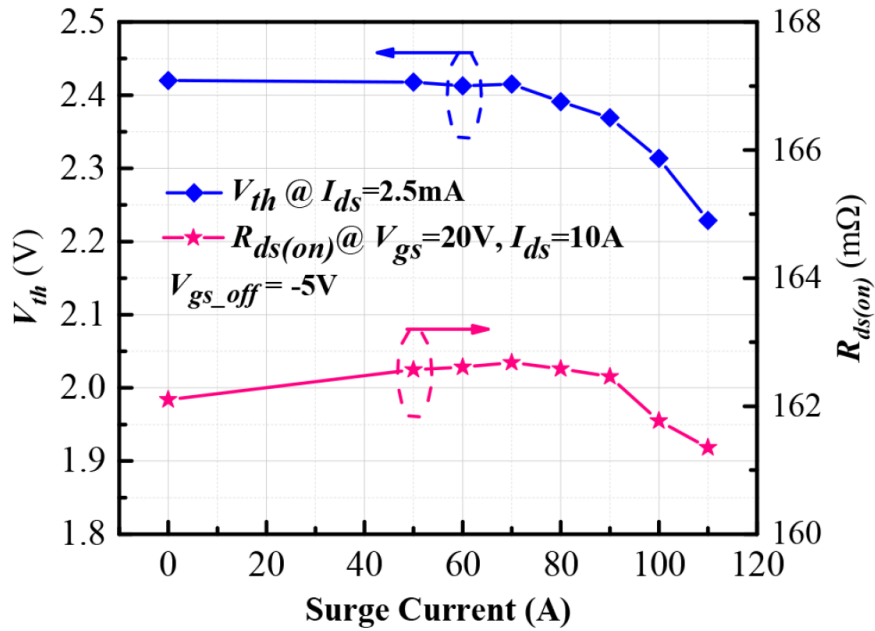


Figure 10 - Evolution of V_{TH} and $R_{DS(on)}$ of 1200 V/12.5 A (C2M0160120D) with the increase of surge current of body diode. Extracted from [30].

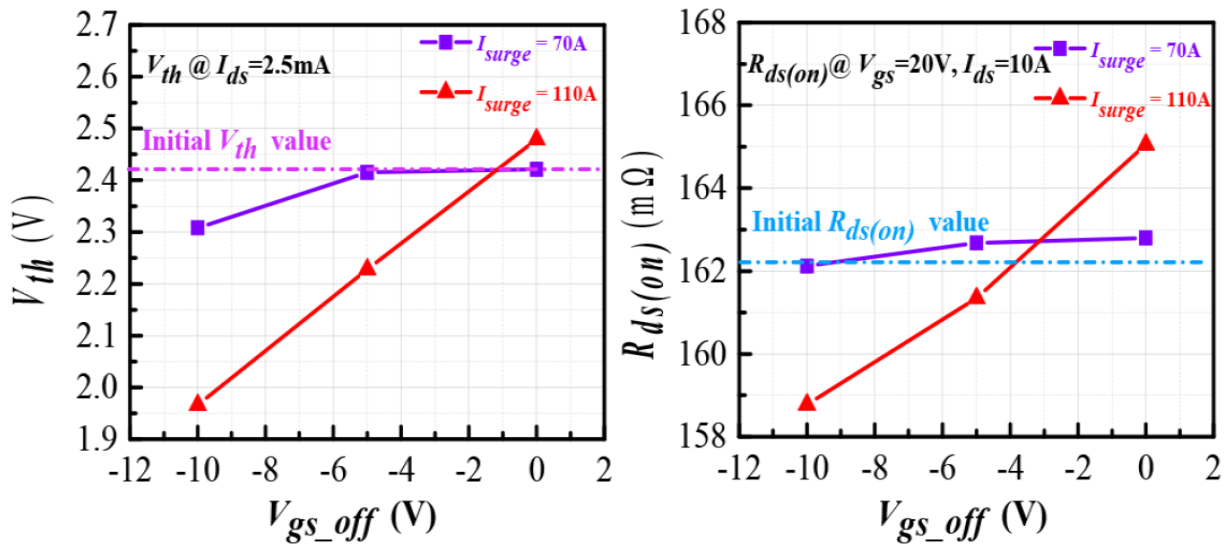


Figure 11 - Evolution of V_{SD} and $R_{DS(on)}$ of 1200 V/12.5 A (C2M0160120D) with different gate turn-off voltage after 70 and 110 A surge current stress of body diode. Extracted from [30].

To provide an example for these ratings, Figure 10 illustrates the evolution of V_{TH} and $R_{DS(on)}$ of a 1200 V/12.5 A (C2M0160120D) SiC MOSFET with varying surge current of the body diode. While the intrinsic body diode of SiC MOSFETs demonstrates excellent surge current ruggedness, noticeable degradation in SiC MOSFETs has been observed after surge current stress [30]. The surge current test method is detailed in [30]. Test SiC MOSFETs underwent 100 cycles of repetitive surge current stress, with periodic measurements of electrical parameters. The degradation of 1200 V/12.5 A (C2M0160120D) planar gate SiC MOSFETs exhibited a strong correlation with surge current amplitude and negative gate turn-off voltage during surge current stress. Figure 10 displays the variation of V_{TH} and $R_{DS(on)}$ after each surge current test. V_{TH} significantly decreases with increasing surge current, while $R_{DS(on)}$ initially increases and then decreases with surge current stress. Figure 11 presents the variation of V_{TH} and $R_{DS(on)}$ with different gate turn-off voltages after 70 A and 110 A

surge current stress of 1200 V/12.5 A (C2M0160120D) planar gate SiC MOSFETs. Both V_{TH} and $R_{DS(on)}$ experience a substantial degradation as the negative gate turn-off voltage decreases. The change in $R_{DS(on)}$ can be attributed to gate oxide degradation, which influences the channel resistance of SiC MOSFETs. The degradation of SiC MOSFETs is primarily caused by charges injected and accumulated within the gate oxide under surge current stress. When the gate turn-off voltage is -5 V and -10 V, the injected holes in the gate oxide lead to a decrease in V_{TH} . Conversely, when the gate turn-off voltage is 0 V, the injected electrons in the gate oxide result in an increase in V_{TH} . To enhance the surge current reliability of the SiC MOSFETs' body diode, an appropriate gate turn-off voltage should be selected to minimize gate oxide degradation induced by potential surge current stress. When the gate turn-off voltage is close to -3 V, a weak electrical field forms along the SiC/SiO₂.

2.2. SiC MOSFETs ruggedness, reliability and aging precursors

Although SiC MOSFETs are qualified and commercially available in the market, further improvements for their ruggedness and reliability are needed in safety-critical applications. In view of this, several conclusions are made based on the review and analyses performed in [34]:

- (i) **SiC MOSFETs have weaker ShC ruggedness than Si IGBTs.** The t_{shc} is significantly influenced by two key factors: the maximum gate drive voltage and the DC bus voltage. Based on this, two distinct ShC failure modes have been identified: gate dielectric breakdown (mode I) and thermal runaway (mode II). The gate dielectric breakdown occurs as a result of the high maximum gate drive voltage, while the thermal runaway failure is caused by high DC bus voltage. It is important to note that the gate dielectric breakdown mechanism in SiC MOSFETs differs from the ShC failure mechanism observed in Si IGBTs. When the maximum gate drive voltage is high, the SiC MOSFET experiences a large saturation current and excessive power loss, leading to elevated junction temperature and melting of the aluminum source metal. Due to the mismatch in coefficients of thermal expansion between different materials in the SiC MOSFET, cracks develop in the gate dielectric layer [75]. Consequently, the melted aluminum metal seeps into these cracks at the upper corner of the MOSFET basic cell, causing a permanent short-circuit between the polysilicon gate and source of the SiC MOSFET. To mitigate the gate dielectric breakdown during ShC stress, it is beneficial to carefully select the source metal. Replacing the aluminum metal with a different metal that has a higher melting point temperature and a smaller coefficient of thermal expansion mismatch between the interlayer dielectric and the source metal can help prevent this failure mode.
- (ii) **Avalanche capability of SiC MOSFETs versus Si IGBTs.** Despite SiC MOSFETs having a significantly higher avalanche energy per area compared to Si IGBTs, their overall avalanche energy is similar to IGBTs due to their smaller chip sizes. It is important to note that the failure mechanism of SiC MOSFETs during avalanche conditions is different from the parasitic BJT latch-up observed in other devices. Instead, the failure occurs when the intrinsic semiconductor temperature limit is reached. Due to this distinction, such tests will not be conducted in SCAPE.
- (iii) **Gate dielectric interface and quality.** Gate oxide defects play a crucial role in determining the reliability of SiC MOSFET chips when subjected to various harsh



operating conditions. Unlike silicon-based devices, gate oxides grown on SiC exhibit a higher density of defects. Following repetitive ShC stress, avalanche stress, or surge current stress on SiC MOSFETs and their body diodes, noticeable degradation in static and dynamic characteristics occurs. This degradation is evident in parameters such as on-state resistance, threshold voltage, drain leakage current, and input capacitances. The degradation primarily stems from interface traps and/or near-interface oxide traps at the SiC/SiO₂ interface. Under stress conditions, these traps capture electrons or holes. The self-heating effect during stress events leads to significantly high junction temperatures in SiC MOSFETs. The elevated temperatures activate additional defects, contributing to an increase in active traps that participate in the charge trapping process. Furthermore, the phenomena of charge tunneling and trapping are sensitive to the applied gate drive voltage and electrical potential on the gate oxide. Higher gate drive voltages and electrical potentials during harsh stress result in more effective charge tunneling and trapping. Consequently, improving the quality of the gate oxide in SiC MOSFETs is a major solution to address ruggedness and reliability issues. Additionally, selecting an optimal gate drive voltage may help mitigate gate oxide degradation in SiC MOSFETs under various harsh stress conditions, including repetitive ShC stress, avalanche stress, and surge current stress.

- (iv) **Degradation in SiC MOSFETs.** In general, the reliability issues of packaged SiC MOSFETs encompass both the degradation of the SiC chip itself and the package surrounding it. When subjected to power cycling tests (PCT), SiC MOSFETs exhibit similar package failure or degradation phenomena as Si devices. These include bond-wire lift-off, heel cracking, and delamination of solder layers. However, the degradation of SiC MOSFETs chips differs from that of IGBTs when exposed to high-temperature PCT stress. This disparity arises primarily due to charge trapping at the SiC/SiO₂ interface, which leads to a significant shift in threshold voltage and forward voltage drop of SiC MOSFETs.

Then, as SiC MOSFETs are intrinsically rugged to UIS events and this condition will not be produced in SCAPE as always an antiparallel diode will be connected, the efforts in SCAPE will be focused towards performing ShC tests on the selected DUTs, detailed further on. In this deliverable, we will center our attention on single ShC I tests and PCT. As for PCTs, the analysis of the degradation at die level will be studied among all selected devices in D3.1 to foresee possible undesired effects in other tasks involving the monitoring of specific electrical parameters monitoring, specially for the digital twin development or state of health analysis during the converter lifetime. Based on the reported results, certain electrical parameters have a potential use as indicators of aging in SiC power MOSFETs at the die-level. These parameters include: gate leakage current (I_{GSS}) [75], [76]; drain leakage current (I_{DSS}) [77]; threshold voltage (V_{TH}) [78], [79]; on-state resistance ($R_{DS(on)}$) [80]; and body diode voltage (V_{SD}) [81]. When compared to Si IGBTs or MOSFETs, the primary differences can be observed in the degradation of the body diode, the changes in threshold voltage caused by charge trapping in the dielectric, and the presence of leakage currents in both the drain and gate. It is important to note that no single parameter can fully explain the degradation or failure of the device, as all them tend to shift due to multiple physical mechanisms rather than a single root cause. Besides, in SiC MOSFETs, both the package and the chip degrade simultaneously, leading to a more complex analysis of the failure mechanism. Therefore, relying solely on a single parameter cannot accurately capture or analyse the underlying physics of these phenomena. Thus, it is necessary to decouple and analyze precursor parameters in a more comprehensive manner to

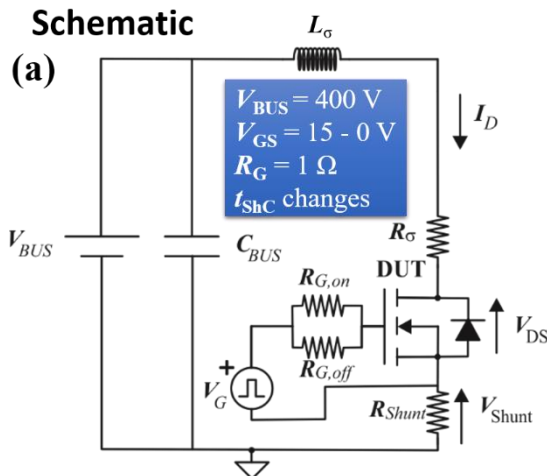


properly exploit them in a final application scenario. This point is intended to be tackled in SCAPE between several tasks of WP5.

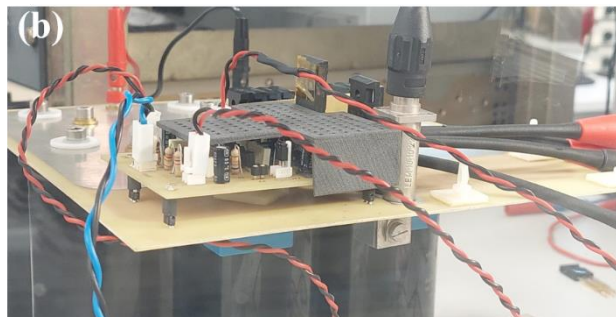
3. ShC I Ruggedness Study

3.1. ShC I setup, experimental conditions and used DUTs

Figure 12 depicts the electrical schematic (see Figure 12a) and the test platform (see Figure 12b) used for ShC I tests, (i.e., Hard Switch Fault condition), also indicating the main parasitic resistance R_{σ} and inductance L_{σ} resulting from the power circuit. This test platform is composed by a DC power supply at V_{BUS} , a capacitors bank (C_{DC}), a gate driver and the DUT. The gate driving is carried out in two separated branches with different gate resistors ($R_{G(on)}$ and $R_{G(off)}$) for turning the DUT on and off. A 10 mΩ coaxial shunt (R_{Shunt}) senses the drain current I_D (V_{Shunt}), whereas two differential voltage probes measure V_{GS} , gate current at $R_{G(on)}$ ($I_{G(on)}$), and drain-source voltage (V_{DS}) in the DUT. The driving conditions (i.e., V_{GS}) depend on the device, and customizable $R_{G(on)}$ and $R_{G(off)}$. Ambient temperature is set for 23°C. ShC I tests are run for each DUT changing t_{on} from 1 μs until reach destruction, while keeping V_{BUS} voltage at 400 V. This value is representative of the voltage sustained by the SC in the final application, as a 3-level converter will be implemented for bus voltage of 1.2 kV. Moreover, $R_{G(on)}$ and $R_{G(off)}$ will be set at 1 Ω, as it is the lowest value to be used in the final converter. These values for V_{BUS} and $R_{G(on)}$ represent the worst-case scenario, as they are the maximum possible voltage rating sustained by the SC under a given ShC and the lowest resistor value to enable the fastest turning on of the device. As for the devices driving, V_{GS} has been set for 15V/0V. All these experimental conditions are also presented in the schematic of Figure 12a.



Experimental Setup



Criterion for actuation time against SCI, $t_{shC} \geq 10 \mu s^*$

*taken from IGBTs for traction in 2000's

Figure 12 – a) Typical ShC I schematic with all parameters described in the text identified. b) Picture of the final implementation of the circuit, remembering the actuation time typically established for Si IGBTs.

As for the DUTs, four kind of samples have been considered according to SiC MOSFETs selected in D3.1. From CREE, 650 V/150 A SiC MOSFETs in TO-247 commercial package (C3M0015065D, called DUT1) and bare die (CPM306500015A, called DUT2) format are used as a devices. Bare dies are packaged at IMB-CNM in TO-247 equivalent format. These SiC MOSFETs correspond to a planar technology, as described in 2.1.1.3, and present an $R_{DS(on)}$ of 15 mΩ. From GENESIC, 750 V/150 A SiC MOSFETs with an $R_{DS(on)}$ of 15 mΩ in bare die format (G4R12MT07-CAU, DUT3) are considered. No details about its internal structure is available and no information can be supplied about its internal characteristics. Finally, from CREE, 1200 V/36 A SiC MOSFETs with an $R_{DS(on)}$ of 80 mΩ in bare



die format (C2M00080120D, DUT4) are also studied to have a reference with a higher breakdown voltage and that can pass the ShC I at the proposed conditions, similar to that presented in [34] but with a higher $R_{DS(on)}$. In this case, this device presents a planar technology.

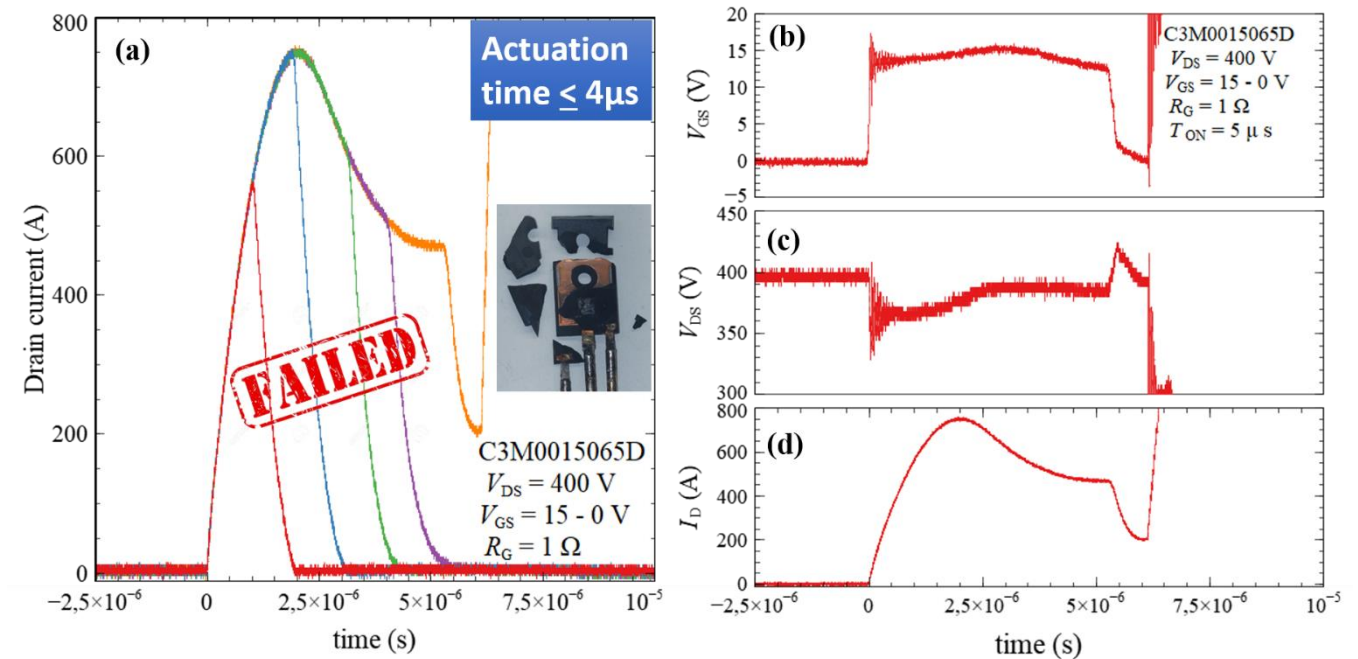


Figure 13 – a) Drain current measured in DUT1 after changing T_{on} from $1\mu s$ until failure, fixing an actuation time of $4\mu s$. All experimental electrical variables measured during ShC I tests when DUT1 failed: b) V_{GS} , c) V_{DS} , d) I_D .

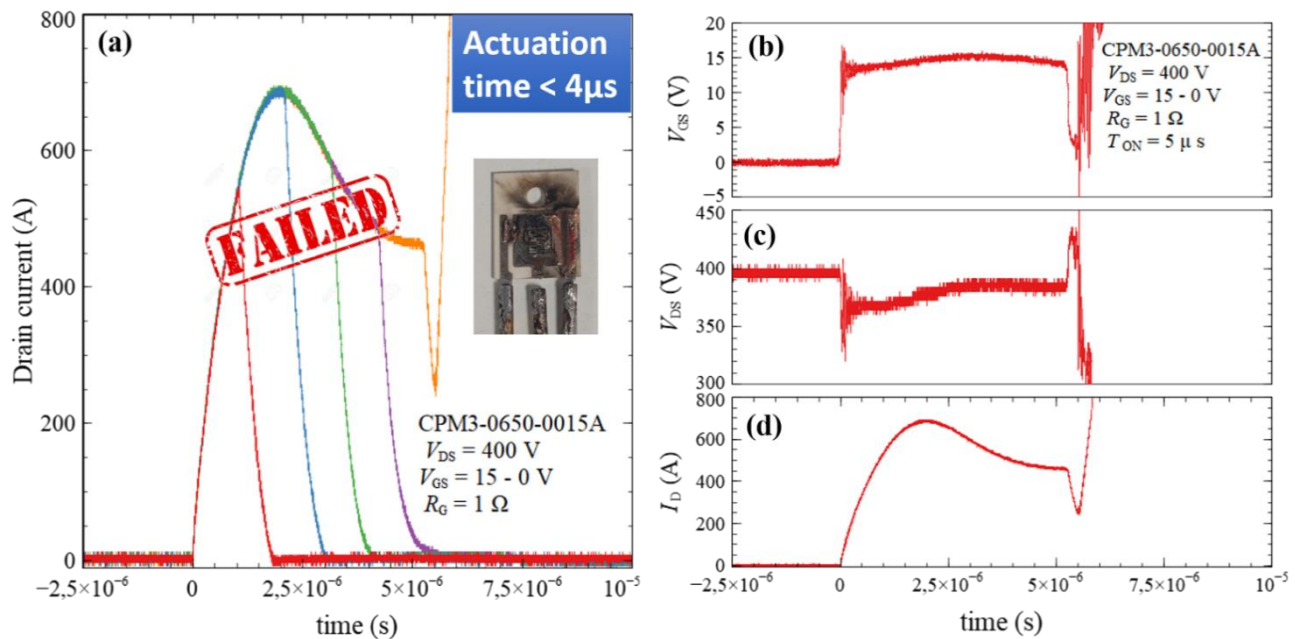


Figure 14 – a) Drain current measured in DUT2 after changing T_{on} from $1\mu s$ until failure, fixing an actuation time of $4\mu s$. All experimental electrical variables measured during ShC I tests when DUT2 failed: b) V_{GS} , c) V_{DS} , d) I_D .

3.2. ShC I Ruggedness tests results and discussion

As for or ShC I tests in DUT1, Figure 13 compares the I_D waveforms obtained during all tests until failure (see Figure 13a) and all electrical waveforms when the device is not capable of withstand a ShC event longer than $10\mu s$, i.e., V_{GS} (see Figure 13b), V_{DS} (see Figure 13c), and I_D (see Figure 13d).

Figure 13a shows that DUT1 has failed for $T_{on} = 5 \mu s$, reaching a maximum I_D value of 750 A. Besides, a picture of DUT1 after failure is presented as an insert. To provide more information about the physics during the failure, Figure 13b, Figure 13c, and Figure 13d are presented. When DUT1 is turned on, V_{GS} starts to slightly increase until I_D reaches a maximum value (first phase). After this point I_D decreases due to high temperature achieved in the channel region resulting from the high dissipation produced in the device. Once I_D has decreased, V_{GS} starts to decrease monotonically until $T_{on} = 5 \mu s$ (second phase). This modulation on V_{GS} is a consequence of high leakage current in the gate due to tunneling effect, driven by impact generated hot holes through the JFET region in the first phase, and after hot electrons due to the high dissipation achieved in the second phase [82]. This is because small gate oxide thickness of the SiC MOSFETs induces a high electric field across the gate oxide and depending on the type of carrier is extracted in the JFET or the channel regions. This carrier transport can be totally enabled by the presence of defects in the dielectric. Some studies have shown that the high temperature associated with high electric fields during a ShC event may damage the thin gate oxide between the gate poly-Si and the 4H-SiC epitaxial layer by means of the tunneling mechanism (failure mode I, see section 2.1.1.1) [82]. Precisely, when V_{GS} decreases, a high component of leakage current due to hot electrons emitted by thermoionic or Schottky processes is produced, due to the high temperature reached close to the dielectric/semiconductor interface [82]. After T_{on} and until failure, V_{GS} shows a sudden slope change due to the discharge of the dielectric, but there is still the high current tunneling due to thermoionic emission. I_D stops decreasing at around 200 A. Due to this, the dissipation becomes very high, the dielectric cracks and the gate leakage current extremely increases, provoking the high V_{GS} increase. Due to the gate control loss, I_D also increases, leading to the melted area observed in the die in the insert of Figure 13a. This burnt out area is homogeneously distributed across the die topside, indicating that the current was homogeneously distributed as well. The variation observed along this process in V_{DS} is a consequence of ShC I parasitics, which drive the first oscillations and the final variation when the device enters into destruction (L_σ and R_σ), while the V_{BUS} decrease is fixed by R_σ . According to this waveforms and the reported literature, the failure is produced in mode I. Notice that in this case, a commercially packaged devices has been analysed. In analogy to DUT1 ShC I results, Figure 14 depicts the ShC I test results for DUT2. Figure 14a presents the I_D waveforms obtained during all tests until failure shows that DUT1 has failed for $T_{on} = 5 \mu s$, reaching a maximum I_D value of 700 A. The waveforms of all electrical significant variables corresponding to the device failure, i.e., V_{GS} (see Figure 14b), V_{DS} (see Figure 14c), and I_D (see Figure 14d), are outlined in the rest of subfigures. Basically, the same results reported for DUT1 have been observed. This means that the ShC I behavior of this component is not totally fixed by the packaging technology itself. It should be pointed out that in the case of DUT2, the failure is produced in a more abrupt manner due to the wirebonding attach locations are so much closer. Thus, more uniform contacts must be distributed and the current symmetry should be optimized in the SCs design. Moreover, a lower current peak is reached during ShC I probably due to a higher series resistance introduced during the packaging process or the variability on $R_{DS(on)}$ resulting from the power device manufacturing process. In any case, the insert of Figure 14a also shows a homogeneously distributed burnt out area across the die topside, indicating that the current was homogeneously distributed when the device exploded.

Figure 15 reports the results for ShC I tests performed in DUT3. Figure 15a plots the I_D waveforms obtained during all tests until failure ($T_{on} = 4 \mu s$, reaching a maximum I_D value of 800 A) and in the insert, the DUT3 after its destruction. The waveforms of all electrical significant variables



corresponding to the device failure, i.e., V_{GS} (see Figure 15b), V_{DS} (see Figure 15c), and I_D (see Figure 15d), are outlined in the rest of subfigures. In comparison to DUT1 and DUT2, some differences can be observed. First, the device has failed in mode I for a shorter T_{on} and a higher I_D maximum value (almost 800A), which establishes an actuation time for the driver shorter than $3 \mu s$. This is normal, as DUT3 presents a lower $R_{DS(on)}$ than the rest of the analysed devices and reach higher dissipation levels faster than the others. As for the waveforms when DUT3 fails, V_{GS} (see Figure 15b), V_{DS} (see Figure 15c), and I_D (see Figure 15d) present a similar behavior. The main difference to DUT1 and DUT2 is in V_{GS} , where leakage current is practically negligible as V_{GS} high level is almost constant. This fact indicates that the quality of the dielectric and its interface with the semiconductor is much better in DUT3 than in DUT1 and DUT2. On the contrary, DUT3 seems to be limited by their internal design, not reaching a noticeable selfheating, as in the case of the other components. This can be observed in V_{GS} (see Figure 15b) and I_D (see Figure 15d). On the contrary to the other DUTs, the insert of Figure 15a reveals that the device topside area is partially burnt out, which points out that the current was not homogeneously distributed when the device exploded. This provide a further improvement to increase the ShC capability for DUT3: a more uniform current distribution should be ensured with an appropriate vias contacts surface distribution across the topside of the device area when packaged with chip-embedding technology. Even the connection tracks should be optimized to ensure this.

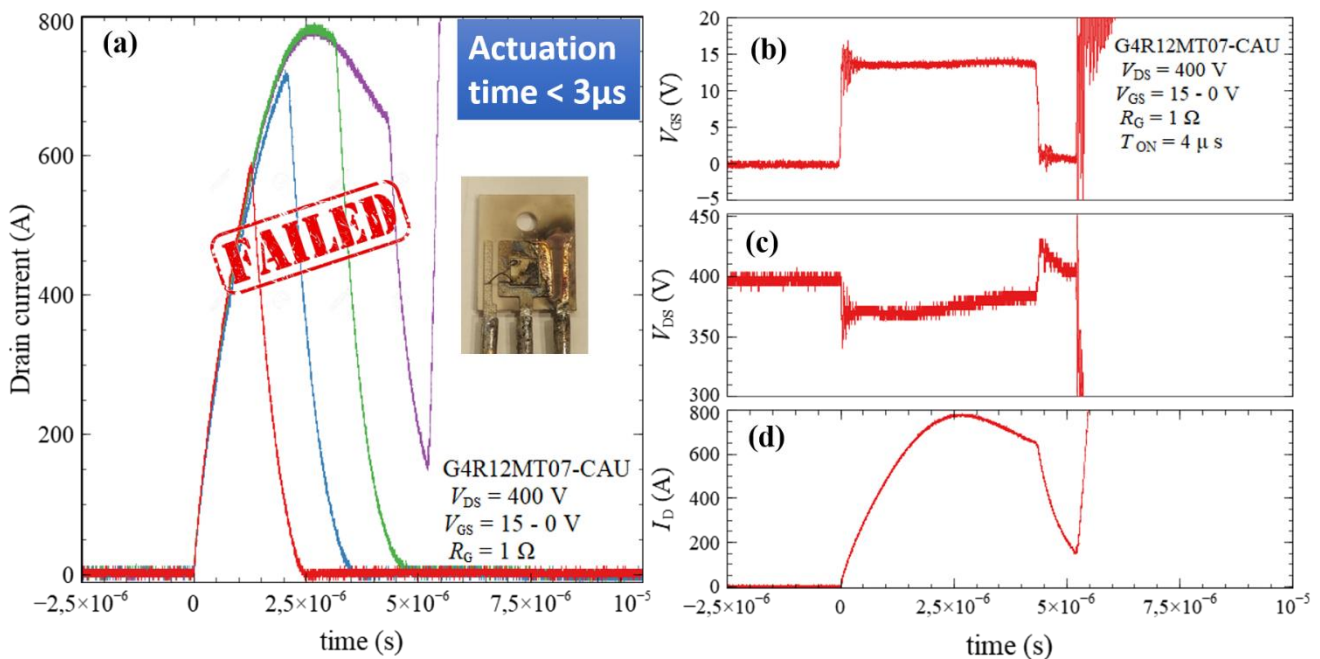


Figure 15 – a) Drain current measured in DUT3 after changing T_{on} from $1 \mu s$ until failure, fixing an actuation time of $3 \mu s$. All experimental electrical variables measured during ShC I tests when DUT3 failed: b) V_{GS} , c) V_{DS} , d) I_D .

Finally, Figure 16 reports the results of ShC I tests performed in DUT4. Figure 16a plots the I_D waveforms obtained during all tests until $T_{on} = 10 \mu s$, reaching a maximum I_D value of 200 A. The waveforms of all electrical significant variables corresponding to the device failure, i.e., V_{GS} (see Figure 16b), V_{DS} (see Figure 16c), and I_D (see Figure 16d), are outlined in the rest of subfigures. As inferred from Figure 16, DUT4 has passed the ShC I tests. Notice that in comparison to DUT1, DUT2 and DUT3, this device presents a thicker drift region (higher breakdown voltage) and in turn, a higher $R_{DS(on)}$. This is why a lower maximum value for I_D is obtained. In addition, the current self-regulation by thermal effects is also well observed in the decay experienced in I_D (see Figure 16a

and Figure 16d). In addition, for V_{BUS} and V_{GS} values considered, the leakage current through the gate is totally negligible, not reaching the same power dissipation levels than in the case of DUT1, DUT2 and DUT3. In spite of the higher $R_{DS(on)}$ values, this device could be a good candidate for being used as i-fuse in SCs, as long as Schweizer technology would be capable of integrating devices with different thicknesses. All results discussed are summarized in Table 1.

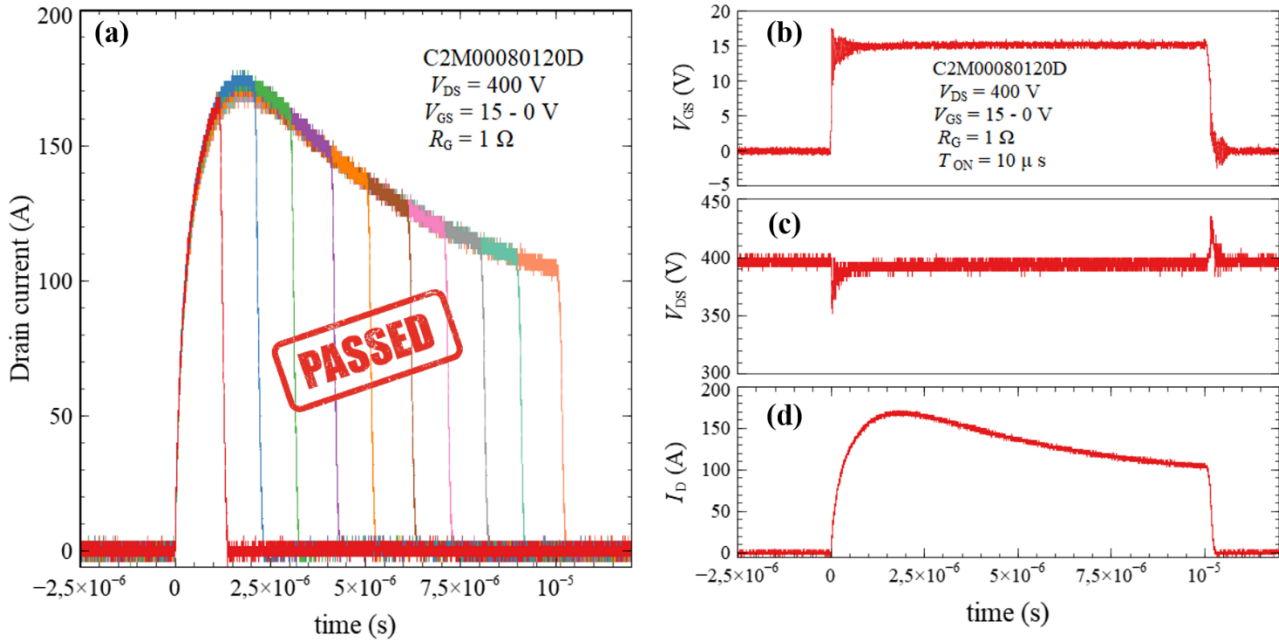


Figure 16 – a) Drain current measured in DUT4 after changing T_{on} from $1\mu s$ until failure, fixing an actuation time of $4\mu s$. All experimental electrical variables measured during ShC I tests when DUT4 failed: b) V_{GS} , c) V_{DS} , d) I_D .

Table 1 – Summary of analysed devices for the ShC I tests.

Part number	V_{br} [V]	$R_{DS(on)}$ [mΩ]	$I_D(@25^\circ C)$ [A]	Actuation time [μs]	Comments
C3M0015065D	650	15	120	≤ 4	<ul style="list-style-type: none"> DUT1: CREE, packaged device Preparation step
CP3M06500015A	650	15	120	≤ 4	<ul style="list-style-type: none"> DUT2: CREE, bare die in C3M0015065D Packaged at CSIC
G4R12MT007CAU	750	12	156	≤ 3	<ul style="list-style-type: none"> DUT3: GeneSiC, bare die Packaged at CSIC Selected device Lowest $R_{DS(on)}$ value Worst ruggedness to ShC I
C2M0080120D	1200	80	36	> 10	<ul style="list-style-type: none"> DUT4: CREE, packaged device Worst $R_{DS(on)}$ value Best ruggedness to ShC I



4. Power cycling study under maximum nominal current conditions

4.1. Power cycling test setup, experimental conditions and DUTs

As previously stated, power cycling tests are performed to induce an accelerated degradation in the package and the device. In this deliverable, a home made equipment has been used to this end. Its schematic and a picture of the test bench are presented in Figure 17a and Figure 17b, respectively. According to the schematic of Figure 17a, an autotransformer (T1) is utilized for adjusting the pulse amplitude, while a second transformer (T2) is responsible for supplying the maximum current required for the test. The test bench has two operational modes: i) Surge current testing mode (switch set to position 2) and ii) Power cycling mode (switch set to position 1). In the surge current testing mode, the current pulse is manually activated by pressing the test button. Each press of the button delivers a 10 ms semi-sinusoidal current pulse to the DUT. The operation principle of the schematic (Figure 17a) is as follows. The "Synchro and Trigger Control" block drives the gate of the thyristor (Ty) at the zero crossing point of the positive slope of the sinusoidal voltage waveform. This signal is synchronized with the test button. The thyristor turns on and remains on until the next zero crossing time of the sinusoidal signal provided by the power supply, after which it turns off. This ensures that only one pulse from the power supply is selected and applied to the DUT. For power cycling, the switch is set to position 1. In this case, the test button is replaced by a low-frequency (1 Hz) oscillator, which controls the operation. The frequency of the oscillator can be adjusted to other values. The DUT is subjected to a high current pulse every second corresponding to a sinusoidal semi-period of 10 ms long, representative of the mains frequency (50 Hz). Each current pulse induces electrical and temperature stress on the device due to self-heating. The device experiences heating and cooling cycles, with the temperature variation dependent on the applied pulse amplitude and the thermal resistance between the device junction and the ambient environment. An electronic pulse counter keeps track of the number of cycles. In this way, this approach enables us monitoring the DUT degradation by analysing the evolution of the voltage drop at high currents as a function of the number of cycles.

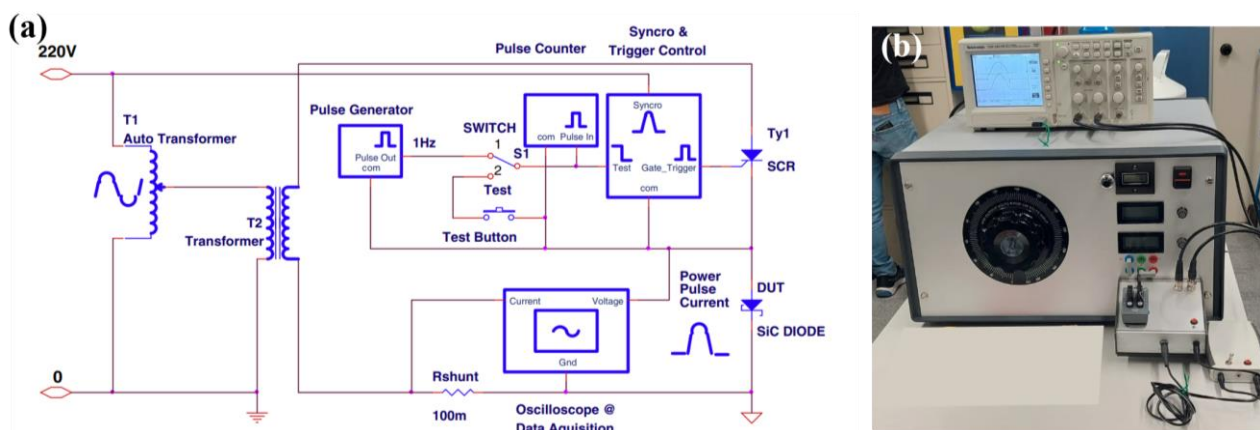


Figure 17 – a) Schematic of the surge current tester. b) Final implementation of the ageing setup.

Here, the proper procedure for power cycling under surge current will not be performed as described in the US Military Standard –STD-750E 4000 Series guidelines, since the preliminary surge current capability tests has not been carried out. To fix the stress current value, the maximum nominal ones given in the datasheets of all studied DUTs have been selected. Then, the maximum values required for the MOSFET (e.g., 120 A) or the diode (e.g., 70A) have been chosen for each DUT, taking into their dimensions and internal structure. Thus, a preliminary study has been performed

with a surge current of 120 A for DUT1 without heatsink (i.e., case temperature $T_c \approx 50-70^\circ\text{C}$) and $V_{GS}=0\text{V}$, setting the device on the third quadrant conduction of its I-V static curve (power cycling test 1, PCT1). In this case, the drift in the following static I-V curves have been used as aging indicators:

- Diode: from an I_D-V_{DS} @ $V_{GS} = 0\text{ V}$;
- MOSFET: from an I_D-V_{DS} @ $V_{GS} = 15\text{ V}$, V_{DS} at high current and from its I_D-V_{GS} @ $V_{DS} = 3\text{ V}$ (DUT1, DUT2), $V_{DS} = V_{GS}$ (DUT3), $V_{DS}=20\text{V}$ (DUT3), the V_{TH} is inferred.

These static curves have been monitored at several intermediate cycles and have been compared with the pristine ones. DUT1 has been selected as it presented the worst dielectric quality and, aside from stacking faults generation in the structure, it is expected to experience a faster degradation under these tests. After this, a more exhaustive analysis has been performed at 70A for DUT1, DUT2 and DUT3 presented in 3.1 using the same aging indicators (power cycling test 2, PCT2). For DUT4, the stress current is reduced to 40A as this is its maximum nominal current. In PCT2, 500 kcycles have been set as a limit to stop the aging if no degradation is observed in the static I-V curves. This value would be increased if it was necessary to explore if any degradation could occur. The rest of conditions have been kept equal than in PCT1 (sinusoidal semi-period 10 ms, etc.).

4.2. Power cycling tests under maximum current nominal conditions: results and discussion

4.2.1. Power cycling test 1

DUT1 has been submitted until observing a severe degradation in one of its aging indicators. The tests have been stopped after 177874 cycles. Figure 18 summarises all aging indicators monitored during the power cycling tests under surge current for each part of the SiC MOSFET, i.e.:

- Diode part: the third quadrant of the I_D-V_{DS} @ $V_{GS} = 0\text{ V}$ (see Figure 18a),
- MOSFET part: I_D-V_{DS} @ $V_{GS} = 15\text{ V}$ (see Figure 18b) and I_D-V_{GS} @ $V_{DS} = V_{GS}$ (see Figure 18c).

In each case, the initial curve (pristine device) is compared to both an intermediate state (95608 cycles) and the final state (177874 cycles) during the tests. Taking this into account, In the case of the degradation in the diode, Figure 18a evidences that a significant V_{DS} drift is observed at 100 A, firstly slightly reducing its value, to eventually be increased at the end of the tests. A more important degradation is observed in the case of the $R_{DS(on)}$, first slightly decreases until see a noticeable and significative reduction after 177874 cycles (see Figure 18b). In the case of the I_D-V_{GS} @ $V_{DS} = V_{GS}$ curves, a threshold voltage variation (ΔV_{TH}) is also observed: from a $\Delta V_{th} < 0$ to a $\Delta V_{th} > 0$. Despite of $V_{GS} = 0\text{ V}$ This is consequence of the charge trapping processes in the channel (in inversion) and JFET (in accumulation) areas. After 95608 cycles, it seems that a higher accumulation of positive charge is trapped in the JFET region, while after hot electrons are captured in the channel region [83]. These results go in line with the conclusions extracted in section 3.2. However, it should be noticed that the conditions we have selected in these first qualification tests are extremely stressful as no heatsink has been used. Therefore, some of the degradation mechanisms that originate these drifts maybe thermally-driven, as for instance the carrier trapping processes observed in the dielectric or at the 4H-SiC/SiO₂ interface. Thus, to really assess the analyzed DUTs, the conditions set for PCT2 will be more realistic for the final application proposed. Moreover, this suggests to also perform an I_D-V_{DS} @ $V_{GS} = -5\text{V}$ to ensure that the channel conduction is turned off.



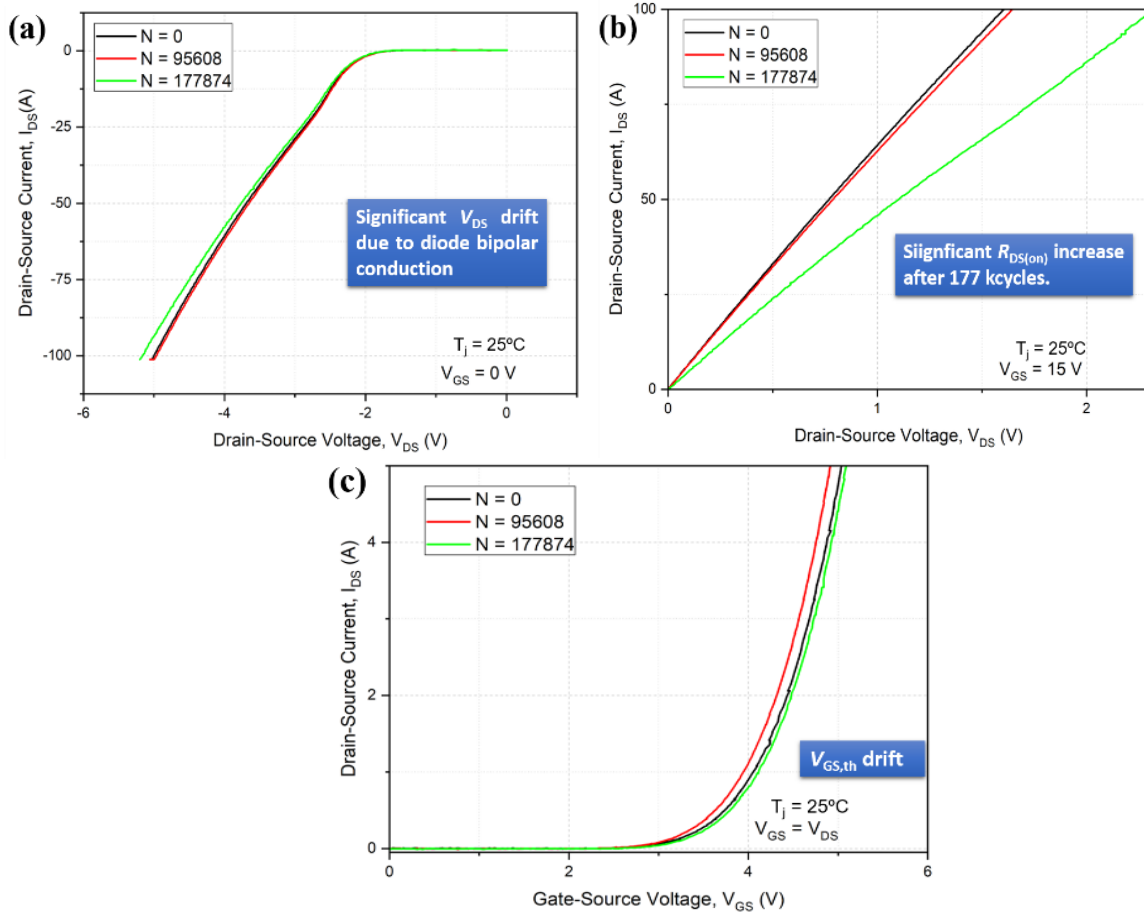


Figure 18 –Degradation of DUT1 according to the following aging indicators monitored at two intermediate cycles: a) I_D - V_{DS} curve @ $V_{GS} = 0\text{ V}$, b) I_D - V_{DS} @ $V_{GS} = 15\text{ V}$, and c) I_D - V_{GS} @ $V_{GS}=V_{DS}$. The junction temperature at the very beginning of the tests was 25°C . No heatsink used.

4.2.2. Power cycling test 2

In these new set of stresses, DUT1 has experienced a lower degradation in comparison to the results presented in 4.2.1., as can be inferred from Figure 19. Figure 19 depicts all I-V static curves used as aging indicators monitored during the power cycling tests under surge current (at cycles 96175 and 50000) for each part of the SiC MOSFET, i.e.:

- Diode part: the third quadrant of the I_D - V_{DS} @ $V_{GS} = 0\text{ V}$ and $V_{GS} = -5\text{ V}$ (see Figure 19a), In this case an additional V_{GS} value is accounted for to decouple the effect of the channel in the degradation process, as at $V_{GS} = -5\text{ V}$ the channel is totally turned off.
- MOSFET part: I_D - V_{DS} @ $V_{GS} = 15\text{ V}$ (see Figure 19b) and I_D - V_{GS} @ $V_{DS} = 3\text{ V}$ increasing the current until 10 A (see Figure 19c). These test conditions have been changed as instabilities have been observed in DUT1 and DUT2 during the characterizations, losing repeatability. This can be due to the interface states along the dielectric and semiconductor. Setting a higher value on the VDS this measurement condition is improved for these devices, being capable of measuring with a good accuracy and repeatability the V_{TH} degradation when it occurs.



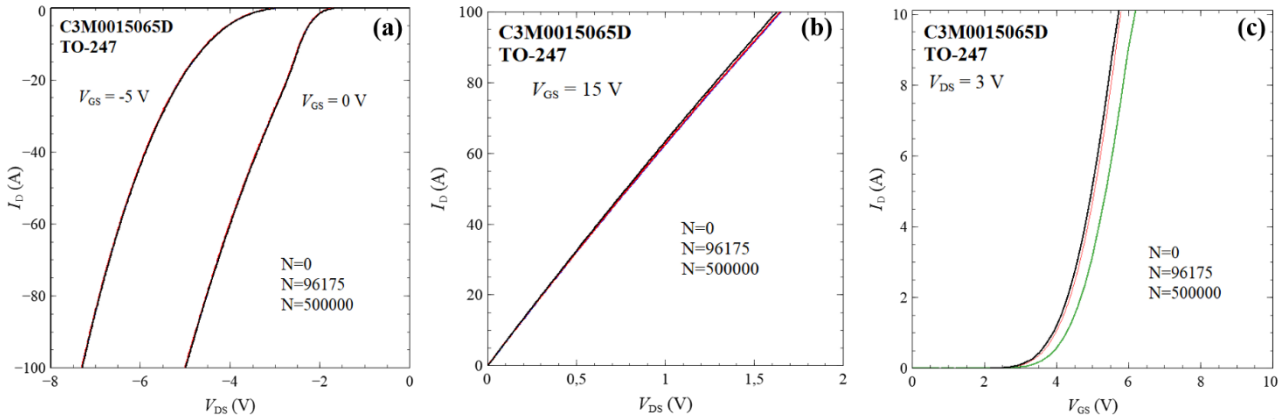


Figure 19 – Degradation of DUT1 according to the following aging indicators monitored at several intermediate cycles: a) I_D - V_{DS} curve @ $V_{GS} = 0$ V and $V_{GS} = -5$ V, b) I_D - V_{DS} @ $V_{GS} = 15$ V, and c) I_D - V_{GS} @ $V_{DS} = 3$ V. The junction temperature was almost kept at 25°C with a heatsink.

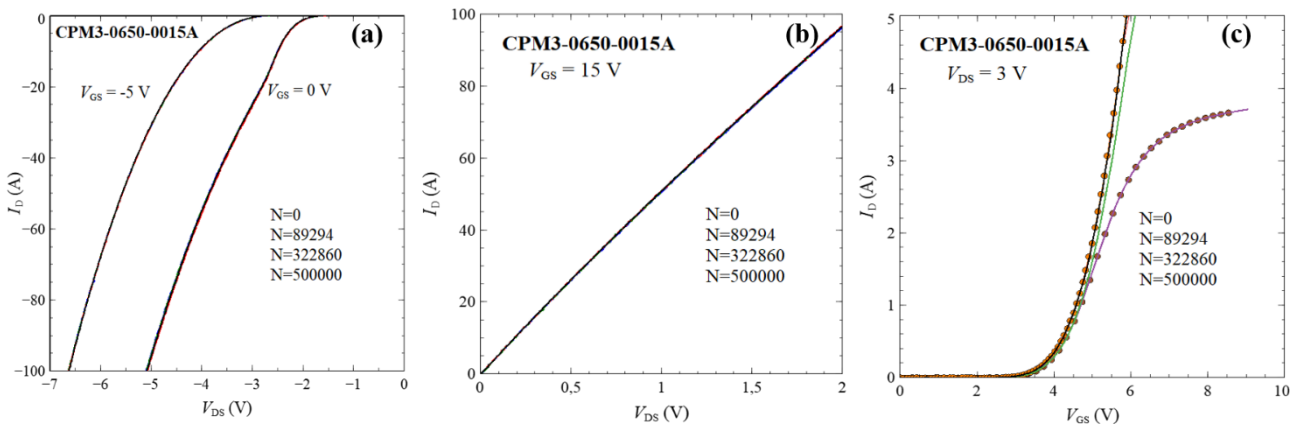


Figure 20 – Degradation of DUT2 according to the following aging indicators monitored at several intermediate cycles: a) I_D - V_{DS} curve @ $V_{GS} = 0$ V and $V_{GS} = -5$ V, b) I_D - V_{DS} @ $V_{GS} = 15$ V, and c) I_D - V_{GS} @ $V_{DS} = 3$ V. The junction temperature was almost kept at 25°C with a heatsink.

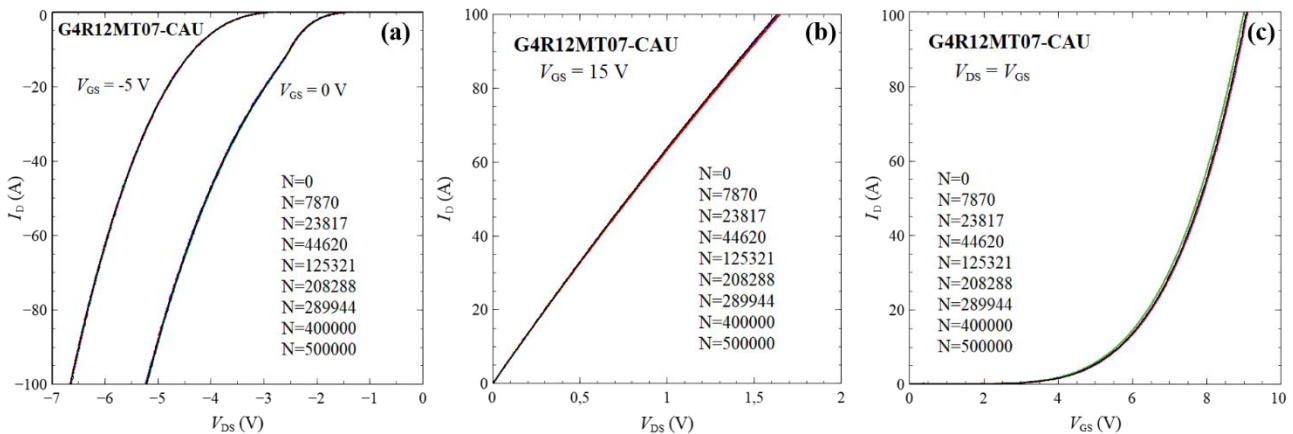


Figure 21 – Degradation of DUT3 according to the following aging indicators monitored at several intermediate cycles: a) I_D - V_{DS} curve @ $V_{GS} = 0$ V and $V_{GS} = -5$ V, b) I_D - V_{DS} @ $V_{GS} = 15$ V, and c) I_D - V_{GS} @ $V_{DS} = V_{GS}$. The junction temperature was almost kept at 25°C with a heatsink.



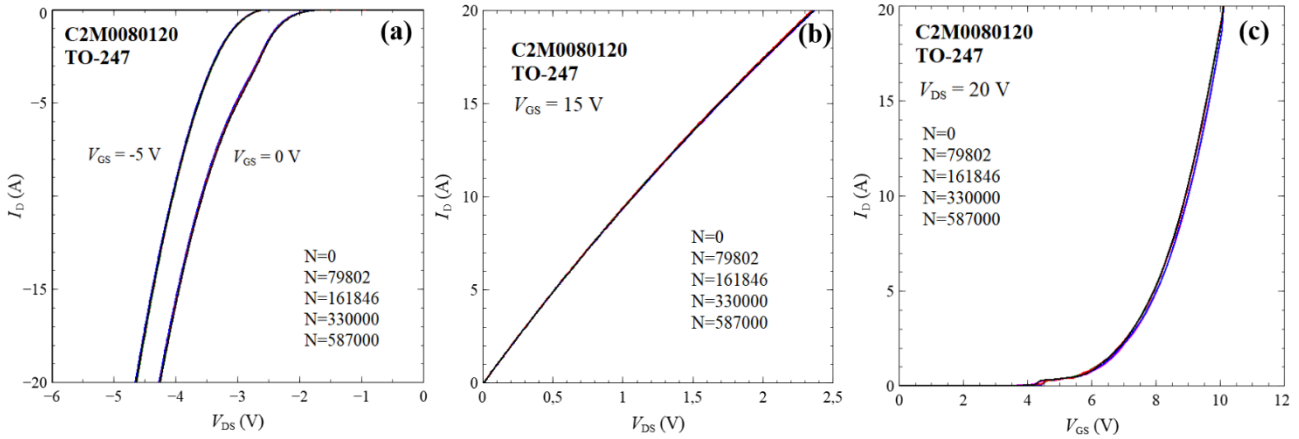


Figure 22 – Degradation of DUT4 monitored at several cycles for the following aging indicators: a) I_D - V_{DS} curve @ $V_{GS} = 0$ V and $V_{GS} = -5$ V, b) I_D - V_{DS} @ $V_{GS} = 15$ V, and c) I_D - V_{GS} @ $V_{DS} = 20$ V until 20A. The junction temperature was almost kept at 25°C with a heatsink.

Table 2 – Summary of analysed devices with their main characteristics for PCT1 and PCT2 tests.

Part number	V_{br} [V]	$R_{DS(on)}$ [mΩ]	$I_D(@25^{\circ}C)$ [A]	PCT 1 I_{Diode} [A]	PCT2 I_{Diode} [A]	Comments
C3M0015065D	650	15	120	120	70	<ul style="list-style-type: none"> • DUT1: CREE, packaged device • Preparation step • Degradation: V_{TH} drift
CP3M06500015A	650	15	120	N.A.	70	<ul style="list-style-type: none"> • DUT2: CREE, bare die in C3M0015065D • Packaged at CSIC • Degradation: V_{TH} drift
G4R12MT007CAU	750	12	156	N.A.	70	<ul style="list-style-type: none"> • DUT3: GeneSiC, bare die Packaged at CSIC • Selected device in D3.1 • Lowest $R_{DS(on)}$ value • No degradation experienced
C2M0080120D	1200	80	36	N.A.	40	<ul style="list-style-type: none"> • DUT4: CREE, packaged device • Worst $R_{DS(on)}$ value • No degradation experienced

The main conclusions extracted from Figure 19 are the following. Figure 19a and Figure 19b does not show an appreciable degradation due to bipolar conduction in the 3rd quadrant and the channel region, as reported in the case Power Cycling test 1. On the contrary, Figure 19c presents a slight variation of V_{TH} during tests, in a similar way as that presented in 4.2.1. As for DUT2, Figure 20 depicts a similar behavior in the monitored curves as aging indicators at cycles 89294, 322860 and 50000: I_D - V_{DS} @ $V_{GS} = 0$ V (see Figure 20a), I_D - V_{DS} @ $V_{GS} = 15$ V and $V_{GS} = -5$ V (see Figure 20b) and I_D - V_{GS} @ $V_{DS} = 3$ V increasing the current until 5 A (see Figure 20c). On the one hand, no significant



degradation due to bipolar conduction in the 3rd quadrant and the channel region (see Figure 20a and Figure 20b, respectively) is measured. On the other hand, an important change on V_{TH} is detected, even setting the device into saturation because of not only the interface states charging/decharging processes explained before, but also a possible degradation of die surfaces. This is an important result to discard these components that will not be packaged in moulding compound format.

In the case of DUT3, Figure 21 presents all the results during and after tests for I_D-V_{DS} @ $V_{GS} = 0$ V (see Figure 21a), I_D-V_{DS} @ $V_{GS} = 15$ V (see Figure 21b) and I_D-V_{GS} @ $V_{DS} = V_{GS}$ (see Figure 21c). In this case, more intermediate cycles have been considered, to extract the maximum information in view of the results obtained with DUT1 and DUT2. In summary, no degradation is observed in each aging indicator. It is worth to point out that again, DUT1 seems to have more robust gate structure than DUT1 and DUT2.

With regards to DUT4, the results obtained after power cycling are outlined in Figure 22. In analogy to the previous DUTs, Figure 22 represents the static $I-V$ curves used as aging indicators, i.e.: I_D-V_{DS} @ $V_{GS} = 0$ V (see Figure 22a), I_D-V_{DS} @ $V_{GS} = 15$ V (see Figure 22b) and I_D-V_{GS} @ $V_{DS} = 20$ V increasing the current until 20 A (see Figure 22c) In general, the same results observed in DUT1 and DUT2 are also reproduced: No apparent bipolar or channel region degradation are observed (see Figure 22a and Figure 22b). In contrast to DUT1 and DUT2, DUT4 does not present any V_{TH} drift (see Figure 22c). It should be noted that this behavior is measured at $V_{DS} = 20$ V until 20A, according to datasheet values, since measurements at $V_{DS} = V_{GS}$ have shown several instabilities even in pristine devices.

All results derived from PCTs are summarized in Table 2. From all analysed devices, DUT3 is the most suited device in terms of gate instabilities, being the most reliable in this sense. Jointly with its low $R_{DS(on)}$, this device is the most interesting for the final application proposed in SCAPE.

5. Conclusions

This deliverable deals with the ruggedness and aging analysis of the power semiconductor devices to be used in SCAPE. Thus, a literature review to identify suitable tests for ruggedness and device aging specific to EV power conversion has been carried out. A critical overview between Si IGBTs and SiC MOSFET devices on their failure physics have been also conducted in this review. As a summary, the following information has been concluded:

- i) SiC MOSFETs exhibit weaker short-circuit (ShC) ruggedness compared to Si IGBTs, with two distinct failure modes identified: gate dielectric breakdown (mode I) and thermal runaway (mode II). To mitigate gate dielectric breakdown, careful selection of the source metal thermomechanical properties is recommended.
- ii) SiC MOSFETs have higher avalanche capability per area than Si IGBTs, but their overall avalanche energy is similar due to smaller chip sizes. The failure mechanism during avalanche conditions is different from parasitic BJT latch-up observed in other devices.
- iii) The quality of the gate dielectric interface is crucial for the reliability of SiC MOSFETs. Gate oxide defects, including interface traps and near-interface oxide traps, contribute to degradation in static and dynamic characteristics. Improving gate oxide quality and optimizing gate drive voltage can help mitigate these issues.



- iv) Reliability issues in SiC MOSFETs encompass both chip and package degradation. Power cycling tests reveal similar package failure phenomena as Si devices, but the degradation of SiC MOSFET chips differs due to charge trapping at the SiC/SiO₂ interface.
- v) SiC MOSFETs are inherently rugged to unclamped inductive switching events. Therefore, efforts in the project will focus on performing short-circuit (ShC) tests and analyzing degradation at the die level.
- vi) Certain electrical parameters, including gate leakage current, drain leakage current, threshold voltage, on-state resistance, and body diode voltage, show potential as indicators of aging in SiC power MOSFETs. However, no single parameter can fully explain degradation or failure, and a comprehensive analysis of precursor parameters is necessary.
- vii) The degradation of SiC MOSFETs involves both the package and the chip, requiring a more complex analysis of the failure mechanism. Therefore, a holistic approach considering multiple parameters is needed for a comprehensive understanding of these phenomena.

Next, the most appropriate tests for multilevel topologies have been selected, adapted to and implemented in the framework of the project. In this sense, ShC tests and power cycling at maximum rated values given in the datasheet have been pointed out as the most significant tests to be performed in SCAPE. UIS tests have been discarded as SiC MOSFETs are intrinsically rugged to UIS events and the intrinsic freewheeling diode is always connected. Finally, from the analysis of the obtained results, several inputs have been provided to other tasks and WPs:

- i) the most suitable SiC MOSFET references for SCAPE have been selected to ensure and improve a high reliability in the converter.
- ii) It is interesting performing ShC I tests at lower DC bus voltage, i.e., VDC= 200V. This value represents a half of the voltage considered in tests reported here and correspond to a realistic value of the bus voltage seen by the component in the final topology selected for the project. These studies were not possible to be included in this report for time schedule. They will be performed before the end of this year.
- iii) Good uniformity in current density should be supplied to final SCs to properly exploit the components capabilities. In this way, ShC I capability can be improved.
- iv) The time withstanding ShC I event has been determined, jointly with the devices degradation.

For efficiency and reliability reasons, devices with better dielectric-semiconductor interface and lower $R_{DS(on)}$ values at nominal operation conditions have been preferred for the final application. For this reason, the GENESIC device (G4R12MT07-CAU, DUT3) has been selected to be used as a switching device. To enable the actuation of i-fuse an leave time enough for its actuation, the CREE, 1200 V/36 A SiC MOSFETs with an $R_{DS(on)}$ of 80 m Ω (C2M00080120D, DUT4) will be a good candidate whether it is compatible with chip embedding process. DUT3 has been desestimated as it presents a higher density of stated in the dielectric and 4H-SiC/SiO₂ interface, as well as stacking faults that degrades the performance of the body diode.



6. Deviations from the work plan

As discussed in the Conclusions section, it was found that conducting ShC I tests at a lower DC bus voltage ($V_{DC} = 200\text{ V}$) is an important assessment step. This voltage value is half of what was considered in the tests discussed in this report and reflects the realistic voltage experienced by the component in the selected final project topology. This will enable to extract longer t_{shc} times than those reported here. Due to time constraints, these studies could not be included in this report. However, they will be conducted and added to an updated version of this deliverable before the end of the year.

7. References

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