



## D5.2 – Ruggedness and aging analysis of the SCs

# SWITCHING-CELL-ARRAY-BASED POWER ELECTRONICS CONVERSION FOR FUTURE ELECTRIC VEHICLES

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**Description:** Report on the ruggedness and aging of Switching Cells (SC's) manufactured in WP4, complementing SC characterization data. Additional ruggedness tests on selected devices are included.



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## Executive Summary

In this deliverable, the ruggedness and aging of the manufactured Switching Cells (SCs) are mainly analyzed. Additionally, further ruggedness and aging tests have been conducted on the selected power device detailed in D3.1 and confirmed from a reliability point of view in D5.1 (i.e., GENESIC device G4R12MT07-CAU). They have consisted in to better adapt Short-circuit type I (ShCI) analysis, making it more representative of the power converter application from the perspectives of device degradation and driver actuation. In this sense, the goals of SCAPE deliverable D5.2 entitled “Switching cells ruggedness & aging analysis” are the following:

- i) At the device level, the following studies have been performed by CSIC:
  - a. ShC I analysis under 200 V bus voltage, as indicated in D5.1 to be closer to final application switching, analyzing more realistic conditions; and
  - b. Die degradation under repetitive ShC I events at 400V, to complement the results obtained in ageing studies performed in surge current configuration, to further confirm the critical design parameters identified in D5.1, i.e., short-circuit actuation time and aging indicators, to ensure a high degree of reliability on the converter.
- ii) At the SC level, the activities focused in ShC I testing and thermal cycling by CSIC and TEKNE are reported:
  - a. Die-level ShC I adaptation to SC's (CSIC),
  - b. Study on possible overvoltage conditions in SCs during ShC I events (CSIC),
  - c. SC's Ruggedness under ShC I (CSIC), and
  - d. SC's thermal cycling performed (TEKNE)

The primary conclusions of this deliverable are as follows: The ShC I tests at a bus voltage of 200V show that the selected device exhibits a ShC I withstanding time of 9  $\mu$ s, which is longer than the 1  $\mu$ s detection time achieved in ShC protection of the driver. The GENESIC device withstands approximately 1000 ShC I events at  $V_{DC}=400V$  with a ShC time of 2.5  $\mu$ s. However, after 1500 events, significant degradation in conduction and forward blocking characteristics is observed, although the gate structure remains mostly unaffected. Overvoltage conditions under ShC I have been analyzed in the selected topology (4x2 SCA 3-level legs), and after circuit analysis assuming steady-state and resistor behavior, the highest voltage sustained is 514V, which is below the breakdown voltage of the selected devices (750V). Thus, the selected component appears robust enough for the intended application. Thermal cycling tests for SC aging have been defined, with a temperature swing between -40°C and 150°C. The component successfully withstands these conditions, with no observed degradation. Additionally, the SC's thermal cycling results indicate no degradation in the selected thermal cycling profile, confirming the reliability of the component under specified thermal conditions.



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## List of Acronyms and Abbreviations

|               |   |                        |                      |
|---------------|---|------------------------|----------------------|
| <b>DUT</b>    | Device Under Test                                 | <b>SC</b>              | Switching cells      |
| <b>EV</b>     | electric vehicle                                  | <b>SCA</b>             | Switching cell array |
| <b>HV</b>     | High-voltage                                      | <b>ShC I</b>           | Short-circuit type I |
| <b>JFET</b>   | Junction field effect transistor                  | <b>Si</b>              | Silicon              |
| <b>LV</b>     | Low-voltage                                       | <b>SiC</b>             | Silicon carbide      |
| <b>MOSFET</b> | Metal-oxide-semiconductor field effect transistor | <b>SiO<sub>2</sub></b> | Silicon oxide        |
|               |   | <b>WBG</b>             | Wide band-gap        |

## List of Variables

|                     |   |                 |  |
|---------------------|---|-----------------|--|
| $C_{DC}$            | Capacitors bank   | $R_{shunt}$     | Coaxial shunt for $I_D$ measurement  |
| $I_{b,sat}$         | Peak saturation current   | $R_{\sigma}$    | ShC circuit parasitic resistance   |
| $I_b$               | MOSFET drain current  | $T_{on}$        | Short-circuit duration, fixed by the circuit                                       |
| $I_{bss}$           | Drain leakage current   | $t_{shc}$       | Short-circuit withstanding time by the dev   |
| $I_{GSS}$           | Gate leakage current  | $V_{br}$        | Breakdown voltage  |
| $L_{\sigma}$        | ShC circuit parasitic inductance  | $V_{BUS}$       | DC bus voltage   |
| $R_{ShC I}$         | ShC I Device equivalent resistance  | $V_{DC}$        | DC bus voltage corresponding to a level of a multilevel converter                  |
| $R_{DS(on)}$        | MOSFET's on resistance  | $V_{DS}$        | Drain to source voltage drop   |
| $R_{G(off)}$        | Gate resistor for turning on the device   | $V_{GS}$        | Gate to source voltage   |
| $R_{G(on)}$         | Gate resistor for turning on the device   | $V_{th}$        | MOSFET threshold voltage   |
| $R_{onsp}$          | Specific on-resistance  | $\Delta V_{TH}$ | Variation of $V_{TH}$ at different gate voltages with increasing ShC stress cycles |
| $(R_{DS(on)})/area$ |   |                 |  |
| $R, R_{SS}$         | Auxiliary SMD resistor controlling driver ShC actuation. $R$ in SCAPE schematics and $R_{SS}$ in the gate-driver circuit data-sheet |                 |  |



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## 1. Introduction

The goals of SCAPE deliverable D5.2 entitled “Switching cells ruggedness & aging analysis” are the following:

- i) At the device level, the following studies have been performed by CSIC:
  - a. ShC I analysis under 200 V bus voltage, as indicated in D5.1 to be closer to final application switching, analyzing more realistic conditions; and
  - b. Die degradation under repetitive ShC I events at 400V, to complement the results obtained in ageing studies performed in surge current configuration,
 to further confirm the critical design parameters identified in D5.1, i.e., short-circuit actuation time and aging indicators, to ensure a high degree of reliability on the converter.
- ii) At the SC level, the activities focused on ShC I testing and thermal cycling:
  - a. Die-level ShC I adaptation to SC’s (done by CSIC),
  - b. Study on possible overvoltage conditions in SCs during ShC I events (done by CSIC),
  - c. SC’s Ruggedness under ShC I (done by CSIC), and
  - d. SC’s thermal cycling performed (done by TEKNE) and degradation analysis (done by CSIC and Deep Concept).

Several aspects among these partial objectives are clarified and explained below:

- i) It is important to note that while D5.1 was focused on high-voltage (HV) semiconductor devices for main SCs (traction inverter, battery charger), SCAPE also involves low-voltage (LV) components for EV auxiliary converters. Since LV converters does not require chip-embedding and are less critical, ruggedness and reliability studies in D5.1 In D5.2 and D5.2 are focused on HV SiC power MOSFETs. Concretely, the best references from deliverable D3.1, .e., CREE C3M0015065D and GENESIC G4R12MT07-CAU, are further analysed as some ruggedness and reliability aspects were not considered in D5.1. This has been identified as a deviation from the workplan, as explained in Section 6.
- ii) Additional ShC I testing on HV SiC MOSFETs are conducted in this deliverable to assess the effect of i-fuse, potential degradations from repeated ShC occurrences, and possible overvoltage situations under such stressful operating conditions. ShC I tests are conducted at a DC Bus voltage ( $V_{BUS}$ ) of 200 V to consider i-fuse connected in series (final configuration in the SC). To analyze degradation, ShC I events at  $V_{BUS} = 400V$  with a ShC withstanding time ( $t_{shc}$ ) of 2.5  $\mu s$  are repeated until any electrical degradation is observed. Besides, a theoretical study about overvoltage stress on SCs induced by ShC I is performed, considering the operation of a leg of a converter based on a 4x2 Switching Cell Array (SCA) 3-level.
- iii) Ruggedness tests in switching cells (SCs) are focused on the semiconductor die, as SiC MOSFETs are the most critical part, without considering the packaging. ShC I is selected as this is the most stressful event that could occur.
- iv) SC thermomechanical aging tests are performed to align with ongoing investigations in SCAPE. The SC thermomechanical assessment was completed based on thermal cycle



availability using the climatic chamber and consistent with approaches used in the literature.

Overall, the main conclusions drawn in this deliverable are the following:

- i) **Single components analysis.** According to new tests defined, the GENESIC G4R12MT07-CAU is rugged enough for this application, according to the following results reported in this deliverable:
  - a. **ShC I tests at  $V_{BUS}=200V$ , considering i-fuse role.** The selected device presents a  $t_{ShC} = 9 \mu s$ , higher than  $1 \mu s$  detection time obtained in the ShC protection.
  - b. **Degradation under non-catastrophic ShC I repetitive events.** The GENESIC device withstands about 1000 ShC I events at  $V_{BUS} = 400V$  with a  $t_{ShC} = 2.5 \mu s$ . After 1500 events, a significant degradation in conduction and forward blocking characteristics is observed, though the gate structure remains mostly unaffected.
  - c. **Ruggedness to ShC I-induced Overvoltage.** Theoretically, this overvoltage condition have been analysed in a leg of a 3-level converter based on a 4x2 Switching Cell Array (SCA). After circuit analysis assuming steady state and resistor behaviour, the highest voltage sustained by a SC is 514 V, which is lower than the sum of the breakdown voltage  $V_{br}$  of two SiC MOSFET devices in series (connection in the SC).
- ii) **SC's Ruggedness to ShC I.** After redesigning the driver protection, SCs passed the test at  $V_{BUS} = 400 V$
- iii) **SC's Passive Thermal cycling.** The tests for SC aging have been defined. A thermal cycling based on a temperature swing between  $-40^{\circ}C$  and  $150^{\circ}C$  is selected. ShC I in SC's for ruggedness analysis performed, properly withstanding this condition. As for SC's passive thermal cycling results, no degradation is observed after 1,000 hours with the selected cycling profile.



## 2. SiC MOSFET's Ruggedness Analysis According to SC's Requirements

### 2.1. ShC I Oriented to SC's Operation: i-Fuse Role and Effect of Repetitive ShC I

#### 2.1.1. Overview

As already stated in D5.1, the ruggedness of SiC MOSFETs against ShC I events is a major concern in power electronics systems, especially in motor driving applications. In a ShC I condition, the Device Under Test (DUT) is activated under faulty conditions, experiencing ShC current and withstanding DC voltage until failure occurs within a certain time ( $t_{ShC}$ ). Under such abnormal operating conditions, the goal is to evaluate whether the ShC I duration ( $T_{on}$ ) is sufficient to detect the ShC condition, initiate shutdown, and prevent converter failures.

In a ShC condition, SiC MOSFETs must withstand high current and DC bus voltage until the protection circuits engage, shutting down the gate control signals. As outlined in D5.1, the SCAPE project centers on ShC I-induced events, with tests conducted to simulate the worst-case scenarios (i.e.,  $V_{BUS}=400V$ ). However, two aspects were not taken into account:

1. On the one hand, the role of the i-fuse in ShC I events has not yet been incorporated into these studies, and a different  $V_{BUS}$  value is needed. In these scenarios,  $V_{BUS}$  should ideally be equally distributed between the i-fuse and the MOSFET during a ShC I event. This approach allows us to calculate a more realistic  $T_{on}$  value and evaluate if the driver can detect and respond effectively. All tests will focus on the semiconductor die itself and following the methodology established in D5.1, excluding packaging effects and SC thermomechanical aspects. In such tests,  $V_{BUS} = 200 V$  will be set up.
2. On the other hand, the degradation of the MOSFET under repetitive ShC I was not analysed. As outlined in D5.1, some drift in the device's initial parameters may be observed under such conditions. To ensure that degradation does not compromise functionality and to assess the device's endurance to multiple ShC I events, a study of repetitive ShC I has been undertaken. This issue can be mitigated by configuring the driver to record the number of ShC I events experienced by the device and to deactivate the SC once reached the maximum number of ShC I events prior to becoming unfunctional for the final application. At this point, redundancy strategies should be performed and a warning signal for premature maintenance should be sent to the final user. To be conservative, such tests will be performed at  $V_{BUS} = 400 V$ , the worst-case scenario identified in D5.1, and  $T_{on} = 2.5 \mu s$  as this value is below the actuation time of the driver ( $3 \mu s$ ).

#### 2.1.2. ShC I setup, experimental conditions and used DUTs

As a reminder, Figure 1 depicts the electrical schematic (see Figure 1 a)) and the test platform (see Figure 1 b)) used for ShC I tests, (i.e., Hard Switch Fault condition), also indicating the main parasitic resistance  $R_{\sigma}$  and inductance  $L_{\sigma}$  resulting from the power circuit. This test platform is composed by a DC power supply at  $V_{BUS}$ , a capacitors bank ( $C_{DC}$ ), a gate driver and the DUT. The gate driving is carried out in two separated branches with different gate resistors ( $R_{G(on)}$  and  $R_{G(off)}$ ) for turning the DUT on and off. A  $10 m\Omega$  coaxial shunt ( $R_{Shunt}$ ) senses the drain current  $I_D$  ( $V_{Shunt}$ ), whereas two differential voltage probes measure  $V_{GS}$ , gate current at  $R_{G(on)}$  ( $I_{G(on)}$ ), and drain-source voltage ( $V_{DS}$ ) in the DUT. The driving conditions (i.e.,  $V_{GS}$ ) depend on the device, and customizable  $R_{G(on)}$  and  $R_{G(off)}$ .



Ambient temperature is set for 23°C. Moreover,  $R_{G(on)}$  and  $R_{G(off)}$  will be set at  $1\ \Omega$ , as it is the lowest value to be used in the final converter. These values for  $V_{BUS}$  and  $R_{G(on)}$  represent the worst-case scenario, as they are the maximum possible voltage rating sustained by the SC under a given ShC and the lowest resistor value to enable the fastest turning on of the device. As for the devices driving,  $V_{GS}$  has been set for 15V/0V. All these experimental conditions are also presented in the schematic of Figure 1 a). More details on the setup are given in deliverable D5.1.

As for the DUTs, only two of the four kind of samples analysed in D5.1 are tested. Our focus is to test the selected devices and use another ones as a reference, in this case the ones that presented a shorter ShC I capability. Basically, From CREE, 650 V/150 A SiC MOSFETs in TO-247 commercial package (C3M0015065D, called DUT<sub>1</sub> in D5.1) and, from GENESIC, 750 V/150 A SiC MOSFETs with an  $R_{DS(on)}$  of 15 mΩ In bare die format (G4R12MT07-CAU, DUT<sub>3</sub> in D5.1) are considered. Both devices present a planar technology.

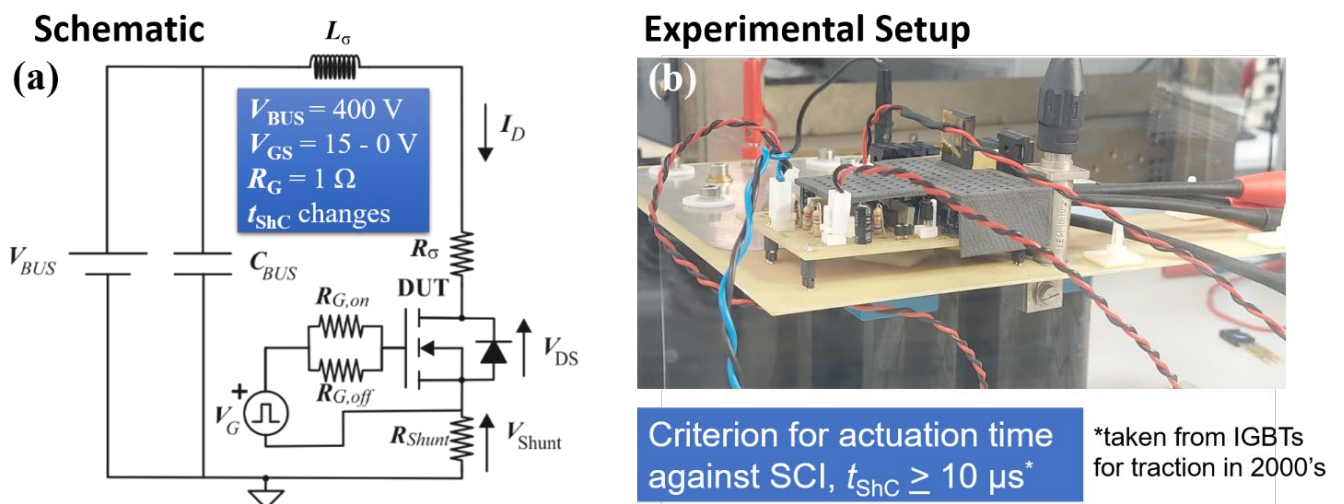


Figure 1 – a) Typical ShC I schematic with all parameters described in the text identified. b) Picture of the final implementation of the circuit, remembering the actuation time typically established for Si IGBTs.

### 2.1.3. ShC I at 200 V of DC bus voltage

As stated, ShC I tests are run for each DUT changing  $t_{on}$  from  $1\ \mu s$  until reach destruction, while keeping  $V_{BUS}$  voltage at 200 V. The results of these tests are depicted in Figure 2, where only the drain current  $I_D$  during ShC I tests are depicted. Moreover, Figure 3 and Figure 4 report the results of ShC I tests at  $V_{DC}=400V$ , corresponding to DUT<sub>1</sub> and DUT<sub>3</sub> and already presented in D5.1. Figure 3 and Figure 4 show all involved electrical variables at the ShC I failure, including:  $I_D$ ,  $V_{GS}$ , and  $V_{DS}$ . Comparing Figure 2 to both Figure 3 and Figure 4,  $t_{shC}$  has become longer. In the case of DUT<sub>1</sub>,  $t_{shC}$  passed from  $4\ \mu s$  to more than  $10\ \mu s$ , while for DUT<sub>3</sub>,  $t_{shC}$  passed from  $3\ \mu s$  to  $9\ \mu s$ . In both cases, a higher margin for actuation under ShC actuation will be available. This confirms that the selected driver is appropriate for this application, whose actuation time under ShC was set in D5.1 to be below than  $4\ \mu s$ .



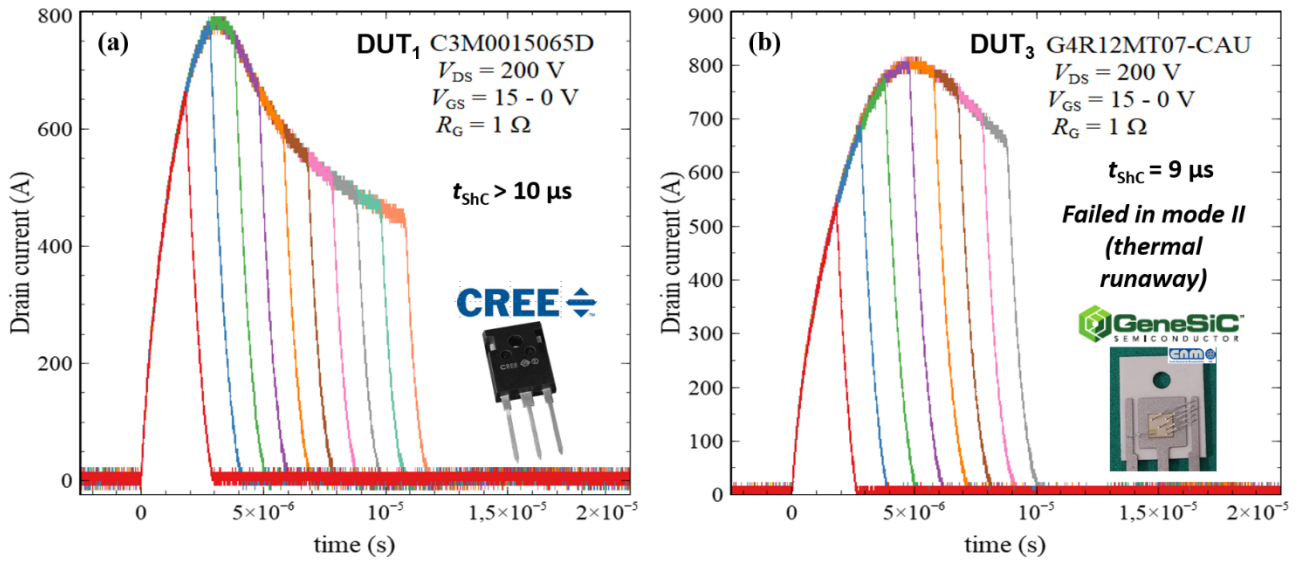


Figure 2 – a) Drain current for DUT<sub>1</sub> showing that  $t_{shc} > 10 \mu\text{s}$ . b) Drain current for DUT<sub>3</sub> showing that  $t_{shc} = 9 \mu\text{s}$ .

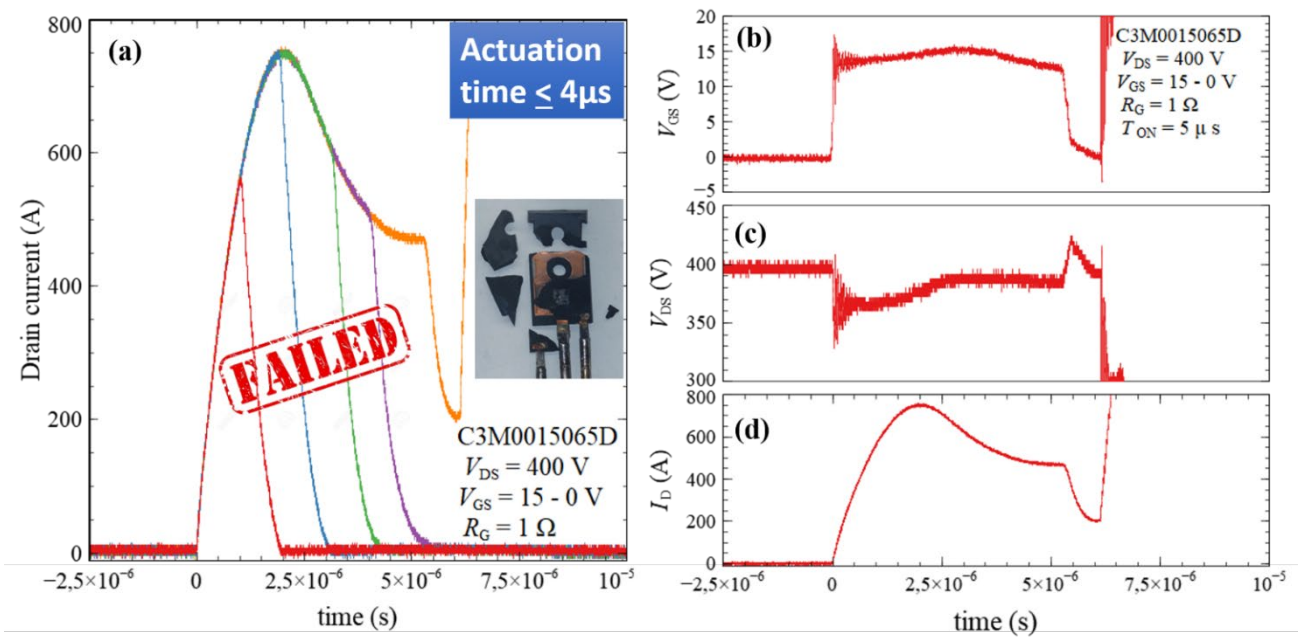


Figure 3 – a) Drain current measured in DUT1 after changing  $T_{on}$  from  $1 \mu\text{s}$  until failure, fixing an actuation time of  $4 \mu\text{s}$ . All experimental electrical variables measured during ShC I tests when DUT1 failed: b)  $V_{GS}$ , c)  $V_{DS}$ , d)  $I_D$ .



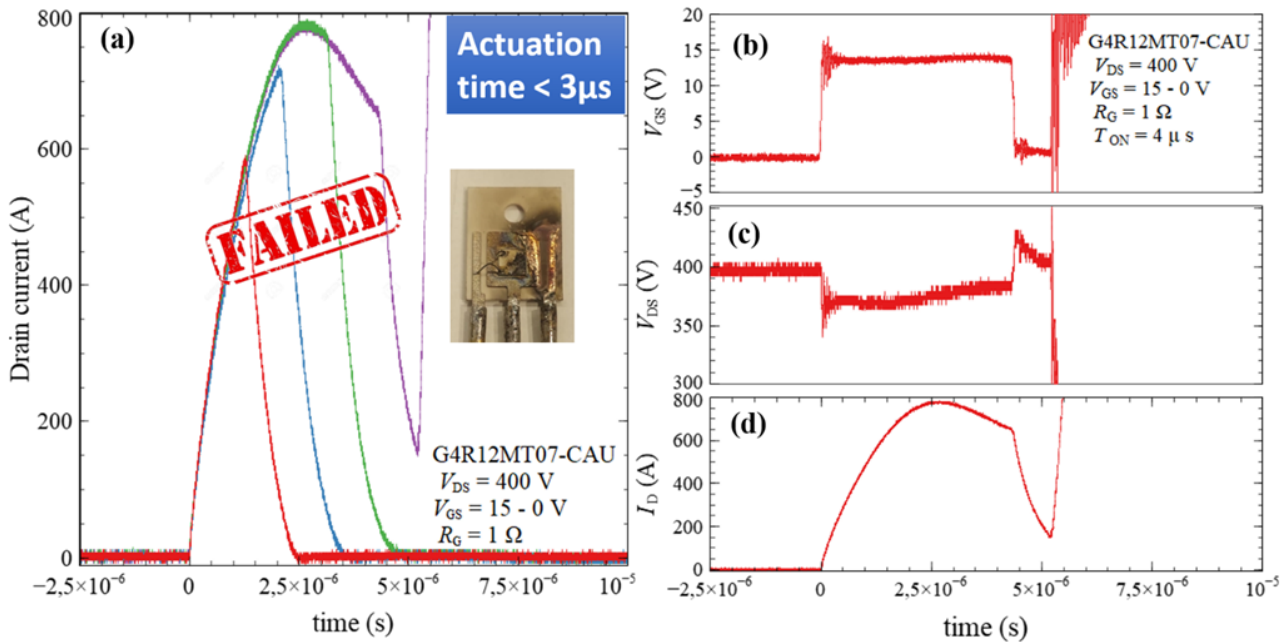


Figure 4 – a) Drain current measured in DUT2 after changing  $T_{on}$  from  $1\ \mu s$  until failure, fixing an actuation time of  $3\ \mu s$ . All experimental electrical variables measured during ShC I tests when DUT2 failed: b)  $V_{GS}$ , c)  $V_{DS}$ , d)  $I_D$ .

#### 2.1.4. Degradation analysis under repetitive ShC I stress

Repetitive ShC I tests are run for DUT<sub>3</sub> keeping  $T_{on} = 2.5\ \mu s$  (shorter than the driver actuation time), while keeping  $V_{BUS}$  voltage at 400 V. Figure 5 depicts the waveforms for the first ShC I performed in the conditions specified above, including  $V_{GS}$  (see Figure 5 a)),  $V_{DS}$  (see Figure 5 b)) and  $I_D$  (see Figure 5 c)). Figure 5 demonstrates the DUT<sub>3</sub> ShC I capability for  $T_{on} = 2.5\ \mu s$ . To provoke a certain degradation, DUT<sub>3</sub> should be submitted until reaching 1513 ShC I events. The electrical parameters which reveal this degradation are  $I_D$  and  $V_{GS}$ . Figure 6 presents such drift in  $I_D$  (Figure 6 a)) and  $V_{GS}$  (Figure 6 b)) after each ShC I for a given number  $N$  of repeated tests. Figure 6 a demonstrates a slight change in  $I_D$ , which is not relevant from an operation point of view. On the contrary, Figure 6 b evidences that  $V_{GS}$  experienced at  $N = 1517$  events a change during the device on conduction and turn-off. During the device on-state,  $V_{GS}$  keeps fixed at 15 V at  $N=1513$ , losing the decrease from 17 V to 16 V. After turn-off,  $V_{GS}$  rapidly stabilises around 0 V when  $N=1513$  is reached, instead of the other case, where  $V_{GS}$  recovers from  $-3\text{ V}$  to  $0\text{ V}$  in approximately 300 ns. To further understand the degradation experienced by the device, the  $I_D$  drift in the I-V static characteristics has been analysed. Figure 7 outlines this analysis comparing the  $I_D$  versus  $V_{GS}$  at  $V_{DS}=10\text{V}$  (Figure 7 a)) and  $I_D$  versus  $V_{DS}$  at  $V_{GS}=15\text{V}$  (Figure 7 b)) before starting tests and after submitting the device to 1513 ShC I events. From Figure 7, it can be inferred the following information. The device threshold gate voltage  $V_{th}$  remains unchanged (see Figure 7 a)). By contrast, the gate leakage current  $I_{GSS}$  slightly decreases, the on-state resistance  $R_{DS(on)}$  and drain-source blocking leakage  $I_{DSS}$  increases significantly. To avoid this drift in the device behavior in final operation, it is concluded that the SC should be deactivated after 1000 ShC I events.

As reported in the literature and reviewed in D5.1, several studies have focused on investigating the effects of long-term or repetitive ShC stress on the static performance of 1.2 kV SiC MOSFETs [1]–[4], which could explain the observed degradation on DUT<sub>3</sub> after ShC I repetitive stress. Various electrical parameters, including  $R_{DS(on)}$ ,  $V_{TH}$ ,  $I_{GSS}$ , and  $I_{DSS}$ , are regularly monitored during ShC pulse stress. It has been observed that  $R_{DS(on)}$  and  $V_{TH}$  exhibit a noticeable increase with the number of ShC cycles in 1.2 kV SiC MOSFETs [4], [5]. This increase is attributed to the melting and reconstruction



of the aluminium surface metallization, which leads to higher  $R_{DS(on)}$ . Additionally, SEM (Scanning Electron Microscope) images of the contact region reveal the formation of significant voids between the aluminium surface metallization and the source contact, resulting in a substantial reduction in the contact interface area [1]. Apart from surface metal deterioration, gate oxide degradation is identified as the primary failure mechanism in SiC MOSFETs under repetitive ShC stress. The shift in  $V_{TH}$  is caused by the trapping of charges in the SiC/SiO<sub>2</sub> interface traps. The concentrated flow of ShC current through the MOS channel generates high temperatures in the JFET region located just below the gate oxide. The most affected area is found along the SiC/SiO<sub>2</sub> interface in the MOS channel region. TCAD simulation results indicate that both the impact ionization rate and the perpendicular electric field in the channel region reach peak values during ShC [5]. The impact ionization generation rate and perpendicular electric field at the SiC/SiO<sub>2</sub> interface are positively correlated with the drain-source voltage. Higher maximum gate voltage and DC bus voltage result in more trapped electrons in the gate oxide. The variation of  $V_{TH}$  ( $\Delta V_{TH}$ ) at different gate voltages with increasing ShC I stress cycles is more significant as the maximum gate voltage is increased, while there is almost no change in  $V_{TH}$  when  $V_{DS} = 0$  V [5]. Therefore, comparing the results reported in Figure 7 a) and Figure 7 b) with those found in the literature, the obtained degradation is more related to the contact degradation rather than that of the SiC/SiO<sub>2</sub> interface. In the case of SiC power MOSFETs with a lower  $V_{br}$  with an hexagonal basic cell, the drift region is thinner and a higher current density is reached, as a lower specific on-resistance  $R_{on,sp}$  ( $R_{DS(on)}/area$ ) is achieved. In our case, this could lead to a higher heat dissipated energy during ShC I events in comparison to their 1.2 kV counterparts, manifesting this degradation in  $R_{DS(on)}$ . By contrast, DUT<sub>3</sub> presents a very stable SiC/SiO<sub>2</sub> interface with no carrier trapping effects, as inferred from the tests performed in D5.1.

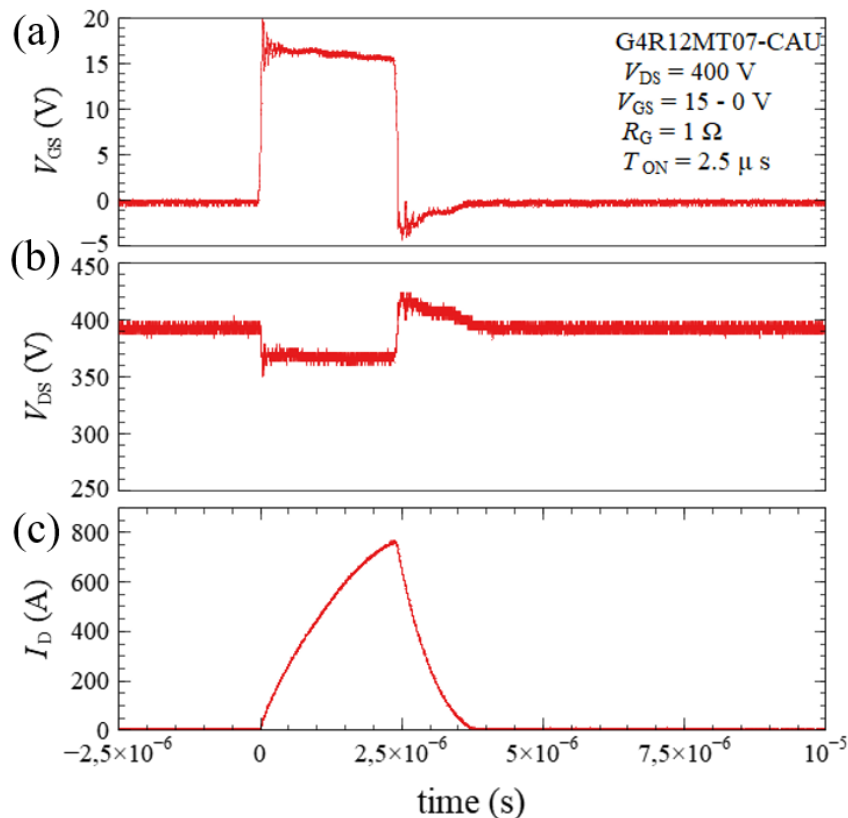


Figure 5 –Fist ShC I experienced by DUT<sub>3</sub>, with the following waveforms: a)  $V_{GS}$ , b)  $V_{DS}$ , and c)  $I_D$ .

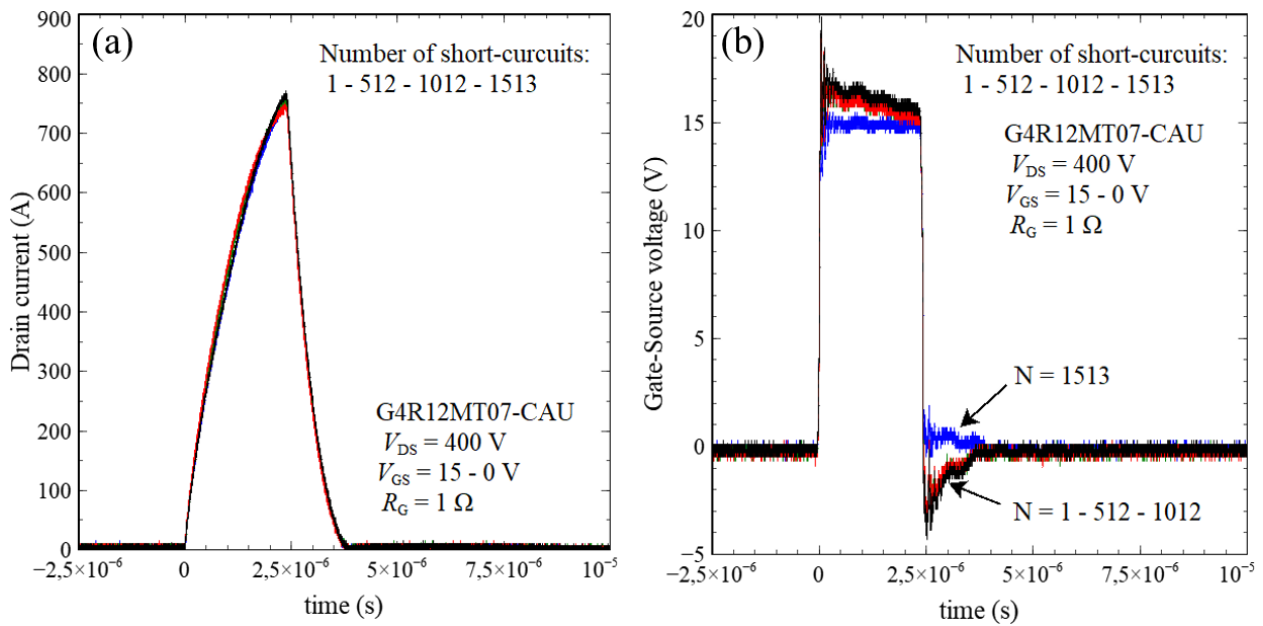


Figure 6 – Changes in electrical variables along 1513 repeated ShC I events: a)  $I_D$  and b)  $V_{GS}$ .

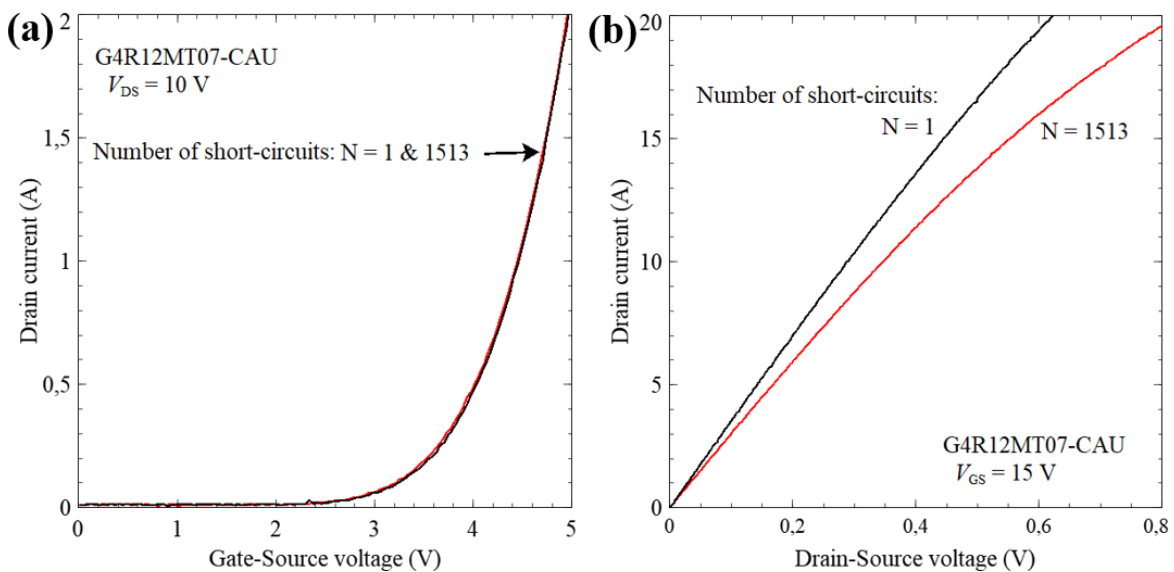


Figure 7 – Analysis of the  $I_D$  drift in the I-V static characteristics : a)  $I_D$  versus  $V_{GS}$  at  $V_{DS}=10V$  and b)  $I_D$  versus  $V_{DS}$  at  $V_{GS}=15V$ .

## 2.2. Overvoltage Analysis after ShC I Event in Final Converters

In this section, the overvoltage seen by some of the SCs is theoretically analysed when one of them enters into ShC I condition. When this abnormal event occurs, one of the SCs is submitted under a higher voltage than the bus voltage for each level  $V_{DC}$ , 400 V. This electrical condition is analysed theoretically with the following assumption: the failed SC has the same equivalent resistance than those ones in conduction mode, and referred to as  $R_{ShC I}$ . To perform a generalistic analysis, the topology with more SCs considered in this project (i.e., 4x2 SCA 3-level legs) will be analysed. To support this analysis, several figures are detailed below. Figure 8 shows the 4x2 SCA 3-level legs when the SC is connected to  $dc_1$  (Level 1),  $dc_2$  (Level 2), and  $dc_3$  (Level 3). With a color code, the SC failed under ShC I condition, jointly with the conduction path enabled, is highlighted under each



situation. For instance, in the case of Level 1, when SC<sub>41</sub> fails (red), the red arrow shows the conduction path between dc<sub>3</sub> and dc<sub>2</sub>. According to Kirchhoff law, the only situations in which overvoltage can occur is when SC<sub>32</sub> enters into ShC I while connected to Level 1, overvoltage is observed in SC<sub>41</sub> or SC<sub>42</sub>, as depicted in Figure 9. The estimated value reached in this case is 514 V, which is lower than the devices breakdown voltage V<sub>br</sub>. The symmetrical situation can be also observed in Figure 9 for the Level 3 connection. In that case, when SC<sub>22</sub> enters into ShC I, overvoltage is observed in SC<sub>11</sub> or SC<sub>12</sub>, reaching the same value as in the prior case. In Figure 10, another overvoltage situation is depicted, where current is conducted by both SiC MOSFET and diode. When connected to Level 2, it takes place when SC<sub>41</sub> or SC<sub>42</sub> enter respectively into ShC I and SC<sub>11</sub> and SC<sub>12</sub> sees the overvoltage. A similar situation is observed when SC<sub>11</sub> or SC<sub>12</sub> fail. SC<sub>41</sub> or SC<sub>22</sub> are the components that see an overvoltage of 457 V.

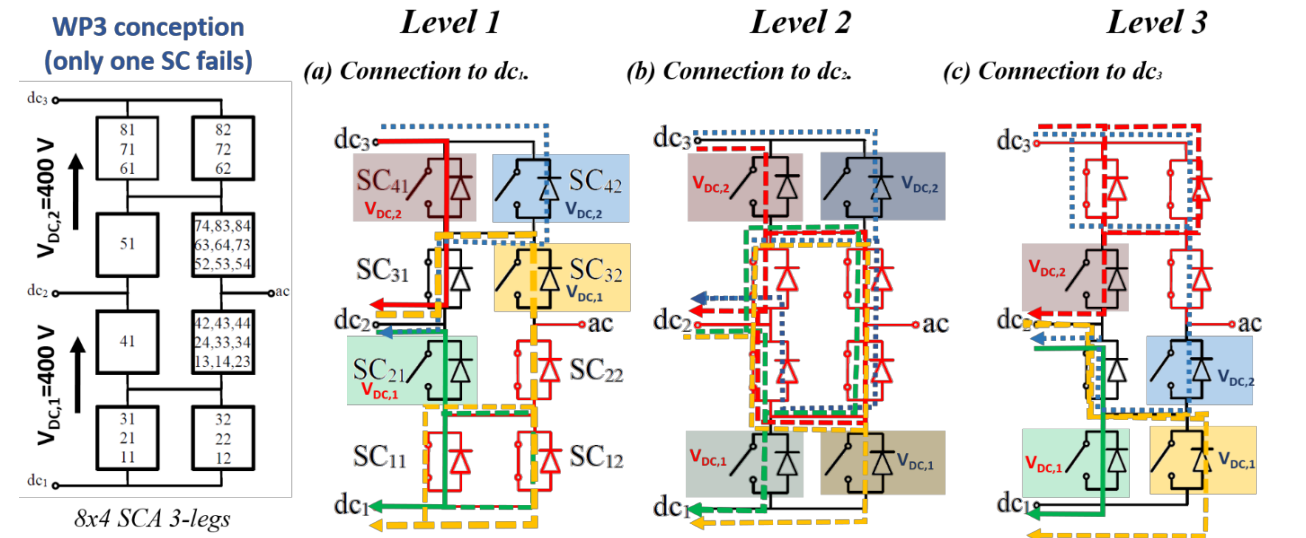


Figure 8 – General overview of the 4x2 SCA 3-level legs: with all different configurations and all paths fixed when one of the SCs fail under ShC I, when connected to levels 1, 2, and 3.

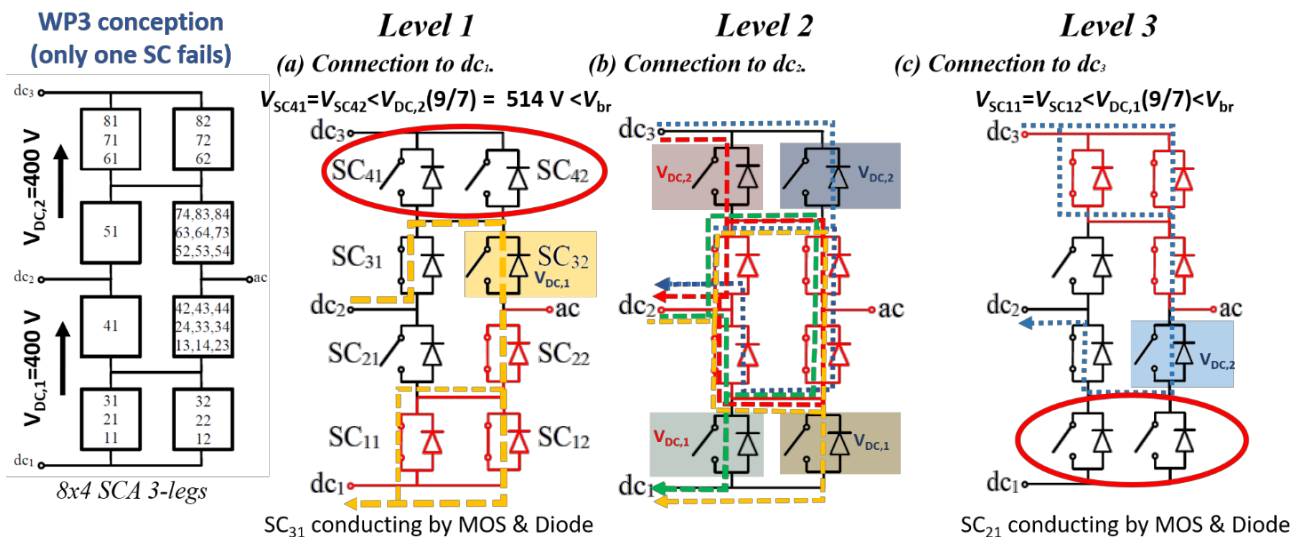


Figure 9 – General overview of the 4x2 SCA 3-level legs: with all different configurations and all paths fixed when the failure under ShC I is: SC<sub>32</sub> fail under connection to Level 1; SC<sub>41</sub>, SC<sub>42</sub>, SC<sub>11</sub> and SC<sub>12</sub> fail connected to Level 2; and SC<sub>22</sub> fails when connected to Level 3

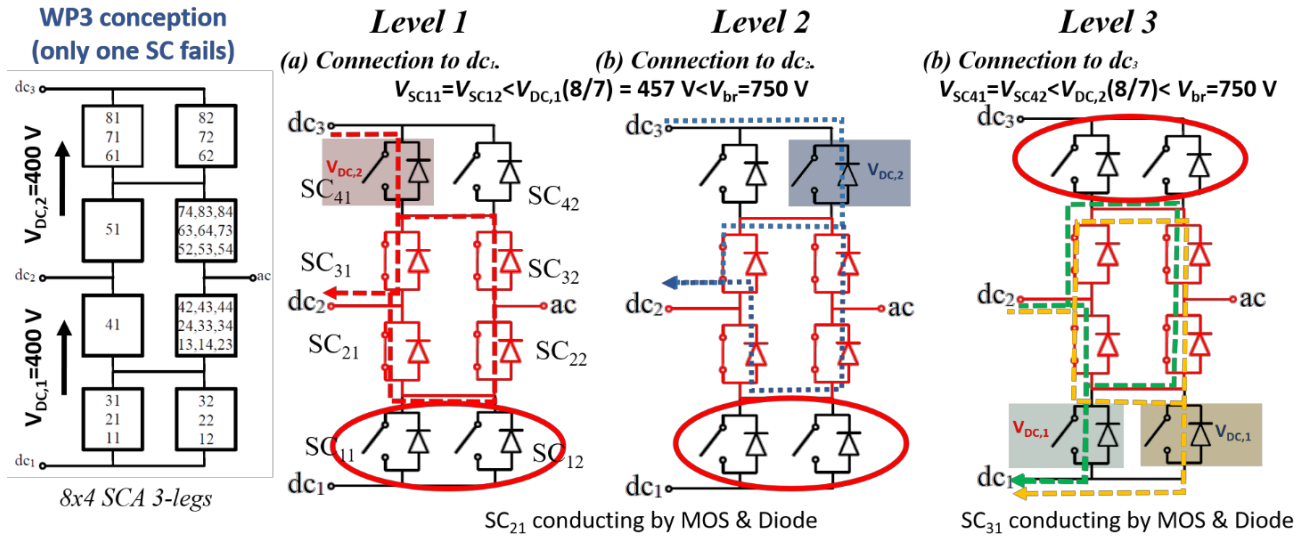


Figure 10 - General overview of the 4x2 SCA 3-level legs: with all different configurations and all paths fixed when the failure under ShC 1 is: SC<sub>41</sub> fails under connection to Level 1, when SC<sub>42</sub> fails connected to Level 2, and SC<sub>11</sub> and SC<sub>12</sub> fails when connected to Level 3



### 3. Switching Cells ShC I Ruggedness Study

#### 3.1. Setup and SC preparation for ShC I studies

The setup for testing ShC I In packaged single devices presented in D5.1 has been used to do the same with the SCs. To connect them to the circuit an interface based on a PCB board has been designed, as Figure 11 demonstrates. Figure 11 a) and b) shows two pictures of the SCs, demonstrating they do not have specific pins to be connected in the ShC I setup. Figure 11 c) to e) display the connection interface between SC and short-circuit test set-up, the ShC I test set-up, and the SC connected to the ShC I set-up after destruction, as it will be explained later.

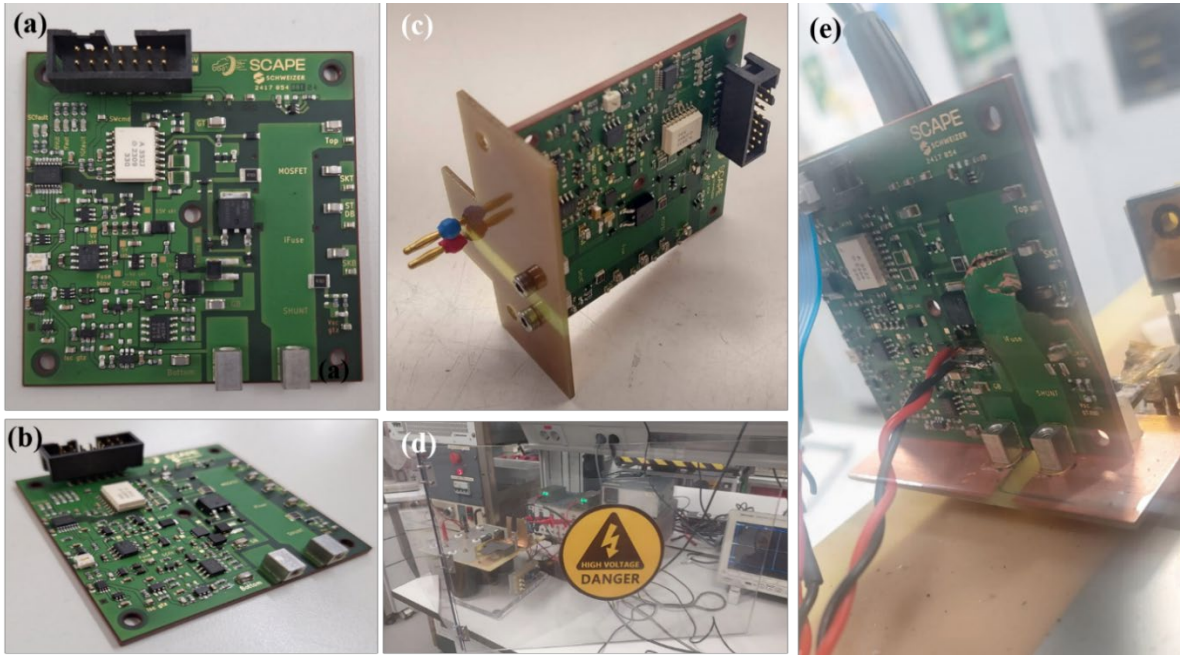


Figure 11 - a) SC top view, b) SC perspective view, c) Interface between SC and short-circuit test set-up, d) Test set-up, e) SC connected to the set-up

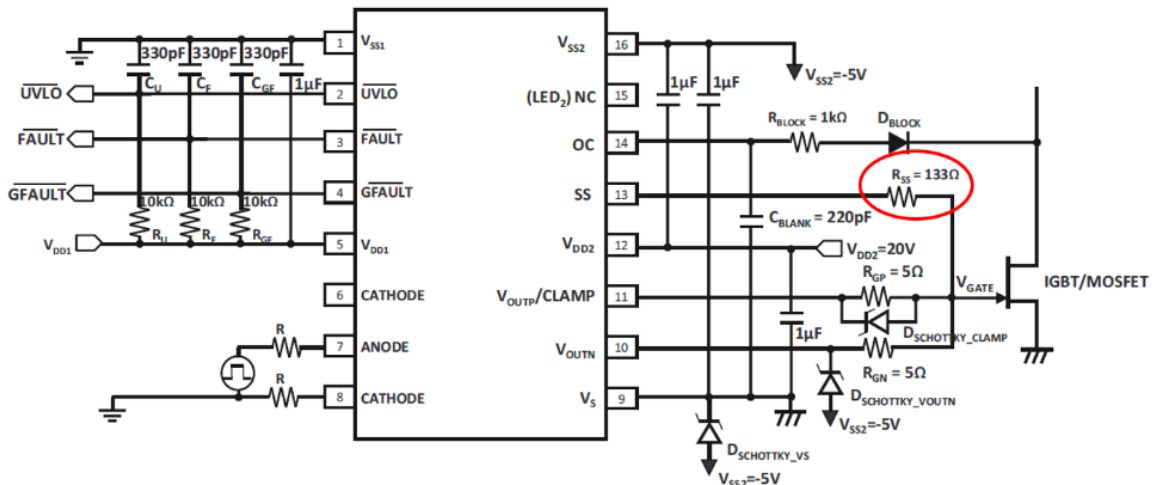


Figure 12 – Driver connections, highlighting the  $R_{SS}$  resistor ( $R$  in SCAPE schematics) and datasheet recommended values.

As for experimental conditions for SCs, the i-fuse is deactivated and the Bus voltage  $V_{BUS}$  will be gradually increased to eventually assess the ShC I protection done with the driver. During overcurrent fault condition, the driver softly shut down the transistor through the SS pin and the

rate of shut down can be adjusted by  $R$ , as indicated in Figure 12. This resistor should be carefully selected to avoid overvoltages in the DC bus sustained by the device under ShC I conditions. A typical datasheet value is  $133 \Omega$ , but to ensure that overvoltage is avoided a higher value of  $330 \Omega$  has been chosen during the SCs design phase in WP3.

### 3.2. ShC I Ruggedness tests results and discussion

The gate driver's protection capability against ShC I for the main MOSFET switch is evaluated and discussed. In preliminary studies conducted in task 5.1, a safe short-circuit reaction time to avoid the destruction of the used SiC MOSFETs of  $2.5 \mu s$  was identified. More details can be found in deliverable D5.1 "Ruggedness and aging analysis of selected power semiconductor devices". That was the starting point for setting up the gate-driver integrated in the SC. The gate-driver detects a short-circuit condition when "high" voltage levels are present simultaneously at the drain and gate terminals. In this case, the gate-to-source voltage  $V_{GS}$  is switched-off with a given delay controlled by an auxiliary SMD resistor, referred as to  $R$  in SCAPE schematics or  $R_{SS}$  in the gate-driver circuit data-sheet. This delay allows a slow current decrease from the short-circuit condition, avoiding critical drain over-voltages. Figure 13 a) shows the waveforms corresponding to 4 short-circuit tests performed on a SC at DC power voltages  $V_{BUS}$  ranging between 100 V and 400 V, for  $R = 330 \Omega$ . As it can be observed, the short circuit current is correctly extinguished for  $V_{BUS}$  between 100 V and 300 V with a current decay time around  $2 \mu s$ . Nevertheless, for a DC power voltage of 400 V, the current suddenly increases without control after its reduction and the SiC MOSFET is completely destroyed due to an excessive over-heating (Figure 13 b)). Fortunately, the SC fails in open-circuit mode, allowing the converter to continue operating correctly thanks to its redundancy capability.

To avoid this effect, the auxiliary resistor  $R$  was reduced to  $62 \Omega$ . Figure 14 presents the main waveforms of a SC that undergoes the same short-circuit tests at  $V_{DC} = 400 V$  for  $R = 165 \Omega$  (see Figure 14 a)) and  $R = 62 \Omega$  (see Figure 14 b)). This figure demonstrates that the safe turn-off time after ShC I is gradually reduced. In the case of  $R = 62 \Omega$ , the short-circuit current elimination takes less than  $1 \mu s$ , avoiding excessive over-heating and the subsequent destruction of the SiC MOSFET. For this case, acceptable overshoots in  $V_{DS}$  are identified (see Figure 14 b)).

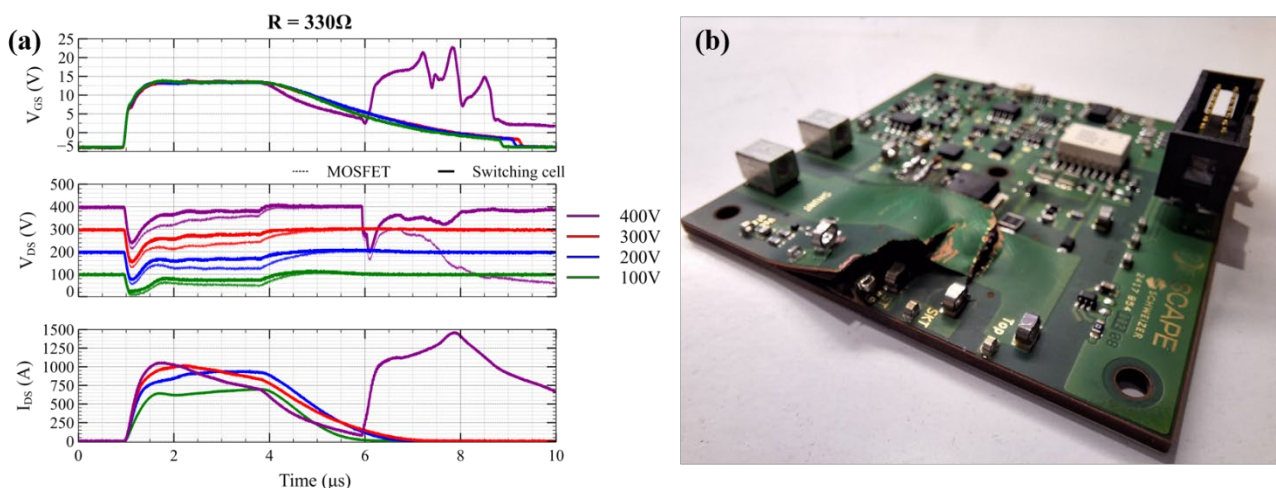


Figure 13 – SC ShC I tests with auxiliary resistor  $R = 330 \Omega$  in the gate-driver. a) Main switch MOSFET drain and gate voltages and current waveforms at different power DC bus voltage (100 V, 200 V, 300 V and 400 V). At 400 V the current dramatically increases after the short-circuit recovery. b) Picture of the SC after destruction of the main switch MOSFET.



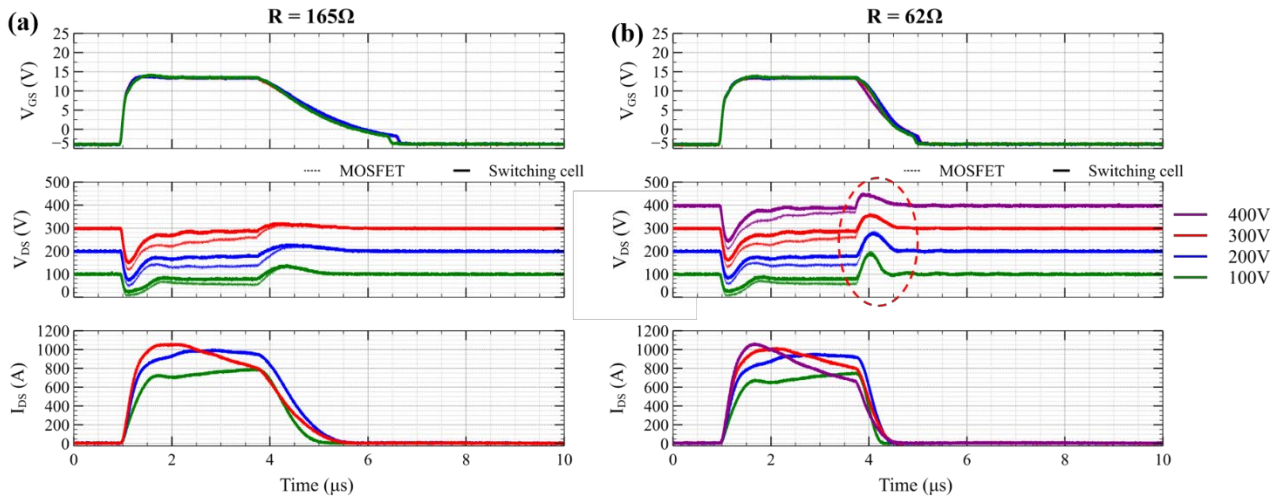


Figure 14 – Repetition of the short-circuit tests with: a)  $R = 165$  and b)  $R = 62 \Omega$ . The SC withstands all the short-circuit events up to 400 V power DC bus voltage.



## 4. Switching Cells Passive Thermal Cycling

### 4.1. Passive thermal cycling setup, experimental conditions and DUTs

As previously stated, power cycling tests are performed to induce an accelerated degradation in SCs. Typically, Schweizer performed thermal cycling tests on its HV-p2-Pack chip-embedding technology based on ICP standards [7]. Our goal in SCAPE is to perform similar aging tests in SCAPE's SC designs looking for their mechanical stability. The thermal cycle is defined combining the temperature range used by Schweizer and the time performances of TEKNE 's climatic chamber. In the TEKNE facilities, an Angelantoni Challenge 250 climatic chamber is available (see Figure 15 a)). This chamber allows for stressing the samples in conditions of high temperature (thermal swing up to 190 ° C) high relative humidity (up to 95%). These conditions are more restrictive than other published in the literature [8]-[9]. The SCs have been located within the climatic chamber as shown in Figure 15 b) so as to force the targeted thermomechanical stress, as depicted in Figure 16. Figure 16 depicts the designed thermal cycle between CSIC and TEKNE. The parameters of the thermal cycle are indicated in Figure 16 a) and the final implementation is provided in Figure 16 b). Figure 16 b) reports a good agreement between the targeted thermal cycle and its final implementation.



Figure 15 – a) Climatic chamber available at TEKNE , and b) SCs situated within the climatic chamber.

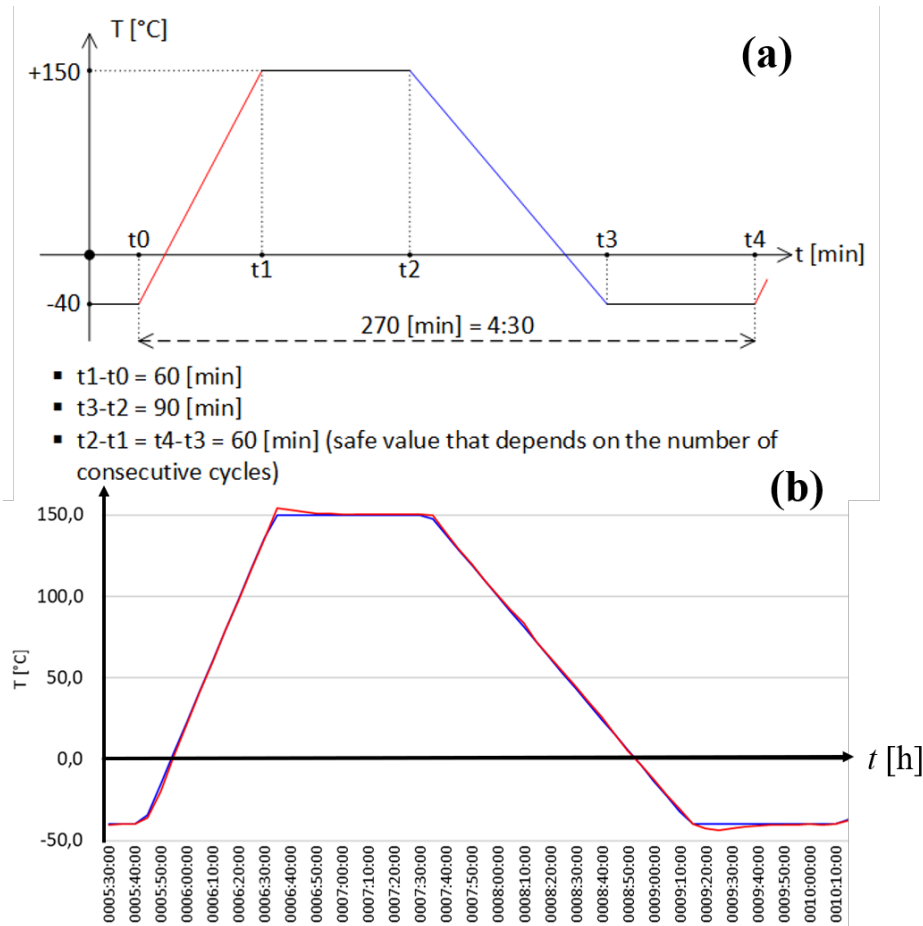


Figure 16 – a) Designed thermal cycle. b) Actual thermal cycle performed in the climatic chamber of Figure 21 a): Ramp-up duration from  $-40\text{ }^{\circ}\text{C}$  to  $+150\text{ }^{\circ}\text{C}$  is 60 min.; ramp-down duration from  $+150\text{ }^{\circ}\text{C}$  to  $-40\text{ }^{\circ}\text{C}$  is 140 min. (it depends on ambient temperature during night and day in a hot month of August), and it stays at  $-40\text{ }^{\circ}\text{C}$  or  $+150\text{ }^{\circ}\text{C}$  during 60 min. Total duration  $\approx 320$  min.

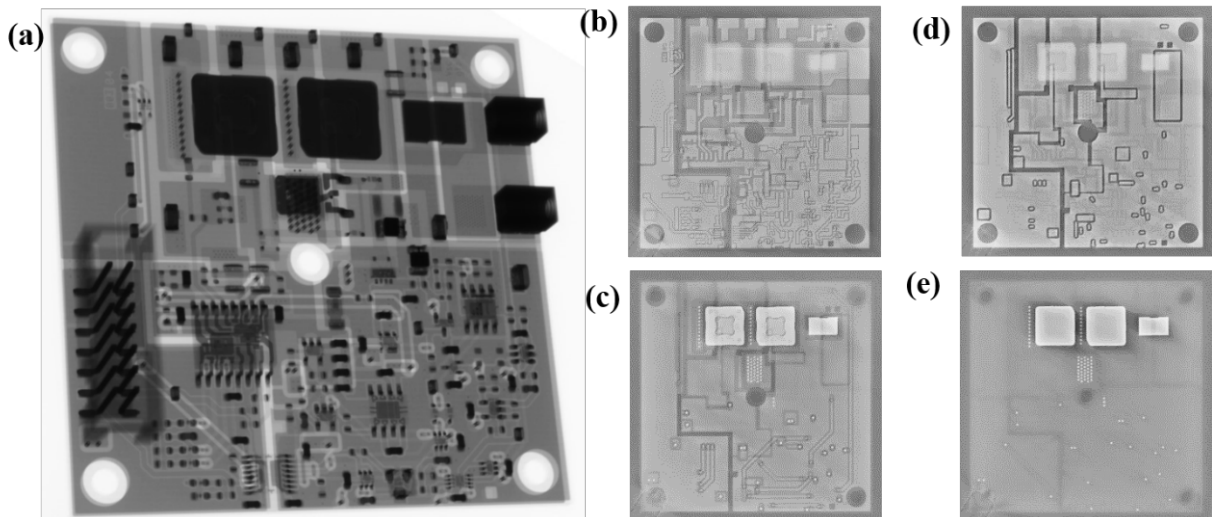


Figure 17 – a) Example of a X-Ray 3D image of one of the boards. b)-e) Example of X-Ray images of a SC focusing at different Z depths for one of the boards, highlighting different elements and interfaces.

Four samples underwent aging for 1000 hours and were labeled as 001-04, 002-04, 003-03, and 003-04. Sample 001-04 was extracted after 168 hours (one week), while the rest underwent 1,000 hours. To prevent potential discharges or electrical issues during thermal cycling, which could



affect the process, they were placed on top of an insulating flexible substrate. Figure 15 b) shows all the samples positioned on the flexible substrate within the thermal chamber.

To inspect and assess the SCs degradation, inspections with Scanning Acoustic Microscope (SAM, Sonoscan Gen-5, [10]) and X rays tomographic system (3DRX, EasyTom S, [11]) have been performed at CSIC and DeepConcept, respectively. Two high resolution techniques to inspect interfaces have been selected. On the one hand, SAM is a sophisticated non-destructive and real-time imaging tool that uses high-frequency sound waves to visualize the internal structures of materials and interfaces without causing damage. SAM operates by emitting ultrasonic waves that penetrate the sample. These sound waves interact with the material and reflect back to the sensor. By scanning the sample with these waves and analyzing the reflections, the microscope creates detailed images of the internal features corresponding to each interface. SAM can achieve high vertical/depth spatial resolution, typically in the range of micrometers or even nanometers, making it suitable for examining small features in various materials. On the other hand, 3DRX systems provide 3D imaging at submicron resolution, allowing for non-destructive examination of complex semiconductor packages using X-rays. It involves rotating an X-ray source and a detector around a sample to capture multiple 2D X-ray images from different angles. These images are then processed using computer algorithms to reconstruct a 3D model of the object. The data collection usually involves hundreds to thousands of X-ray projections, which contribute to a comprehensive dataset for reconstruction. Both techniques are complementary. Thus, SAM allows for interface characterization by ultrasounds and having access to immediate interfaces below the inspected surfaces. In turn, 3DRX allows for a fast view of the full 3D structure of any material. Then, SAM inspections will be targeted to inspect the delamination in the power devices embedded within the PCB, while 3DRX will focus on analyzing the state of degradation corresponding to the tracks and solders of the components on top of the SC and the top part of the embedded power devices. An example of a 3D thomography for the analysed SCs is shown in Figure 17. Figure 17 provides the X-ray view of the whole SC (see Figure 17 a)) and all the different layers (see Figure 17 b)-e)), highlighting all internal tracks or leadframes.

## 4.2. Thermal cycling results

SAM inspections from the PCB backside (main heat-exchange area) have been performed to detect delaminations or defective vías. Special attention has been payed to observe whether there was delamination in the insulation layer present below the dies. After performed analysis, it has been concluded by CSIC the following; No significant degradation is detected after cycling during 1000 hours, as Figure 18 supports. Figure 18 demonstrates that the thermal cycle followed by the samples has not introduced any critical degradation affecting thermal performances of the SC.

After proceeding with the X-ray analysis, these are the main conclusions extracted by Deep Concept and summarised in Figure 19. No delamination or cracks were detected in the solder or between any layers, and all geometries appear intact. Due to the very thin dimensions, achieving 100% inspection certainty is challenging. The complex copper edges introduce artifacts that complicate the X-ray analysis. However, the silver sintering layer on the die-attach remains intact, with no visible cracks.

According to the performed experimental analysis and after all these analyses, no degradation has been experienced by SCs after being submitted under thermal cycles of Figure 16 b).





## 5. Conclusions

The main conclusions drawn in this deliverable are the following. As for ShC I tests at  $V_{DC}=200V$ , the selected device presents a  $t_{shc} = 9 \mu s$ , higher than the  $1 \mu s$  detection time obtained in the ShC protection. The GENESIC device withstands about 1000 ShC I events at  $V_{BUS} = 400V$  with a  $t_{shc}= 2.5 \mu s$ . After 1500 events, a significant degradation in conduction ( $R_{DS(on)}$  increase) and forward blocking characteristics is observed, though the gate structure remains mostly unaffected. This sets a condition for the converter control: after 1000 ShC I events, SC should be deactivated and redundancy strategies should start. Overvoltage conditions under ShC I have been analysed in the selected topology. After circuit analysis assuming steady state and resistor behaviour, the highest voltage sustained is 514 V, which is lower than the  $V_{br}$  of both components (active switch and i-fuse). The selected component seems to be rugged enough to be used in the present application. Thermal cycling tests for SC aging have been defined. A thermal cycle based on a temperature swing defined between  $-40^{\circ}C$  and  $150^{\circ}C$  is selected. ShC I in SC's for ruggedness analysis performed, properly withstanding this condition. As for SC's thermal cycling results, no degradation is observed with the selected thermal cycling profile.

## 6. Deviations from the work plan

As discussed in this report, two ruggedness tests at device level could not be conducted in D5.1 and are finally provided in D5.2. Firstly, it was found that conducting ShC I tests at a lower DC bus voltage ( $V_{BUS} = 200 V$ ) is an important assessment step. This voltage value is half of what was considered in the tests discussed in D5.1 and reflects the realistic voltage experienced by the component within the SC. This will enable to extract longer  $t_{shc}$  times than those reported in D5.1. Secondly, an effective study on repetitive ShC I events was not conducted, as it was discarded at that moment. We realized that this information is key for an effective driving and deactivate the SC when a certain number of repetitive ShC I events are reached.

This deliverable was submitted two months late, with no negative impact on the project's progress. The original due date (31/08/2024, M26) was revised to 31/10/2024 (M28). The delay was due to two factors: (1) a late start of the switching-cell thermal cycling tests at TEKNE facilities, caused by delays in preparing the required climatic chambers, and (2) a notified delay in SC manufacturing. The tests were completed by the end of M26, after which time was needed to finalize the deliverable. The impact is expected to be minimal, as individual switching-cell subsystems were already tested and validated by UPC. The remaining subsystems are straightforward to implement and should function as expected, avoiding the need for rework or remanufacturing. More comprehensive tests will be conducted in Task 7.1 and reported in D7.1.



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